NASA SP-5972 (06)
August 1975

TECHNOLOGY UTILIZATION

# DISPLAYS, MEMORIES, AND SIGNAL PROCESSING

## A COMPILATION


NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

# Foreword

The National Aeronautics and Space Administration has established a Technology Utilization Program for the dissemination of information on technological developments which have potential utility outside the aerospace community. By encouraging multiple application of the results of its research and development, NASA earns for the public an increased return on the investment in aerospace research and development programs.

Compilations are now published in one of nine broad subject groups:

SP-5971: Electronics - Components and Circuitry
SP-5972: Electronics Systems
SP-5973: Physical Sciences
SP-5974: Materials
SP-5975: Life Sciences
SP-5976: Mechanics
SP-5977: Machinery
SP-5978: Fabrication Technology
SP-5979: Mathematics and Information Sciences

When the subject matter of a particular Compilation is more narrowly defined, its title describes the subject matter more specifically. Successive Compilations in each broad category above are identified by an issue number in parentheses: e.g., the (03) in SP-5972(03).

This Compilation contains articles on electronics systems and techniques. The first section is on displays and other electro-optical systems; the second section is devoted to signal processing. The third section presents several new memory devices for digital equipment, including articles on holographic memories.

Additional technical information on items in this Compilation can be requested by circling the appropriate number on the Reader Service Card included in this Compilation.

The latest patent information available at the final preparation of this Compilation is presented on the page following the last article in the text. For those innovations on which NASA has decided not to apply for a patent, a Patent Statement is not included. Potential users of items described herein should consult the cognizant organization for updated patent information at that time.

We appreciate comment by readers and welcome hearing about the relevance and utility of the information in this Compilation.

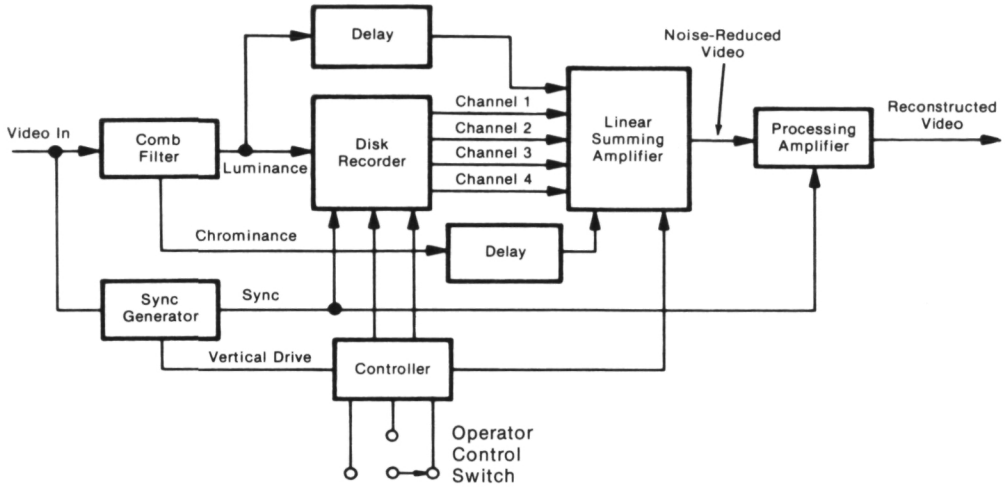


For sale by the National Technical Information Service, Springfield, Virginia 22161

# Contents

# Section 1. Electro-Optical Systems and Displays

## TELEVISION NOISE-REDUCTION DEVICE




Television Noise-Reduction Device

Color-television video signals transmitted in noisy environments produce poor images. Standard filtering techniques to reduce the noise content of video signals usually lead to loss of picture resolution.

A new system has been developed for improving the signal-to-noise ratio in color-television video signals. The system consists of a luminance-chrominance separator, a disk recorder, a summing amplifier, a control device, and a processing amplifier, as shown in the figure. The system divides the color video signals into luminance and chrominance components. As the chrominance signal is sensitive to time-base instabilities, it is not processed and is preserved as is. The sync generator strips the synchronizing signals from the video input and generates its own synchronizing signals, which are applied to the recorder for control of its servo-mechanism.

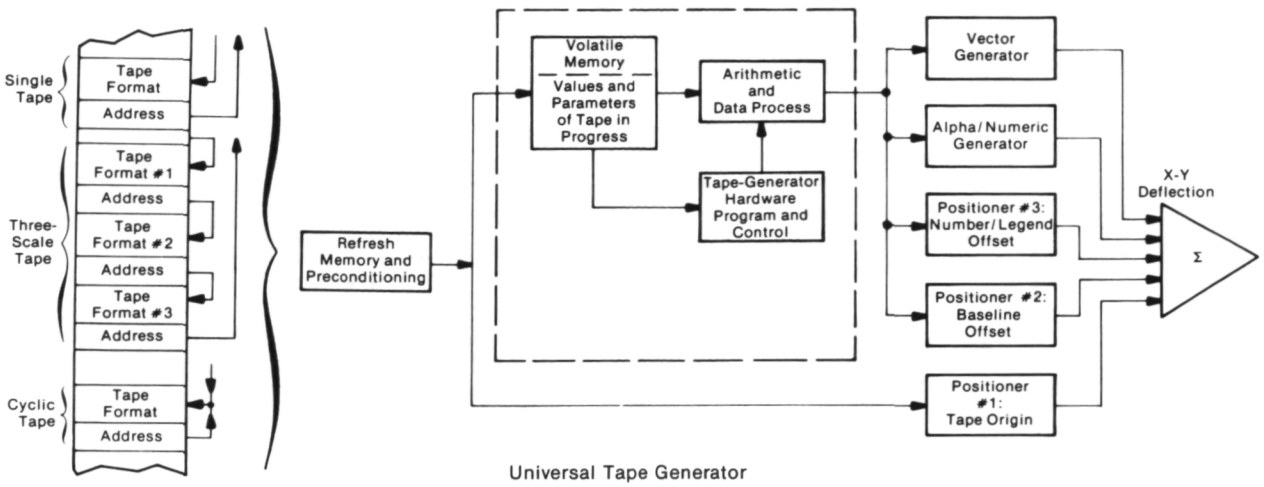
The luminance signal is recorded continually on the disk recorder for a total of four recorded television frames. The luminance signal then is summed also with the previously-recorded luminance signals in the summing amplifier and averaged, so that the signal level is the same as the original luminance signal. The chrominance signal then is added to the new luminance signal, and the result is a noise-reduced television signal. The processing amplifier then is employed to restore synchronizing signals and reference a 3.58-MHz color subcarrier. The controller, which obtains its reference from the sync generator, generates the necessary logic control commands to the disk recorder and the weighting commands to the summing amplifier.

The system greatly improves the signal-to-noise ratio with little or no loss in picture resolution. By storage of the luminance component, which is summed with the chrominance component, the system performs mathematical integration of the basically-repetitive television signals. This integration of the signals over the interval of their repetition causes little change in the original signals and eliminates random noise.

Source: J. C. Stamps
Johnson Space Center and
B. L. Gordon of
Taft Broadcasting Corp.
under contract to
Johnson Space Center
(MSC-12607)

*Circle 1 on Reader Service Card.*

# UNIVERSAL TAPE GENERATOR




Universal Tape Generator

Tapes and scales are frequently used elements of display system symbology. In stroke-written displays, tapes are constructed as a sequence of vectors and alpha/numeric characters which are correctly positioned and scaled.

The universal tape generator is an information retrieval system which is useful for producing simulations on a cathode-ray tube (CRT) display. It consists of a means of storing and retrieving information relating to formats which are to be used in conjunction with the display. With the tape generator, the fixed-format restriction is overcome by the programable definition of tape parameters. The system defines a computational approach which translates programed parameters into display instructions. Specifically included are:

a. The derivation of the first tick-vector starting point and value,
b. The derivation of subsequent tick-vector starting points and values,
c. The derivation of the final tick-vector starting point and value,
d. The derivation of number/legend offsets, and
e. Multiple-scaled and cyclic tape techniques.

A tape is visualized as an arbitrarily long (vertical or horizontal) sequence of ticks which behaves in some cyclic manner with legends and number values displayed at regular intervals. Only a segment or window of this total tape is selected for display. The window is designated by a word representing the tape value at the left (bottom) extreme of the displayed segment. The variety of tape formats is restricted only by word-length limits and the particular set of parameters available.

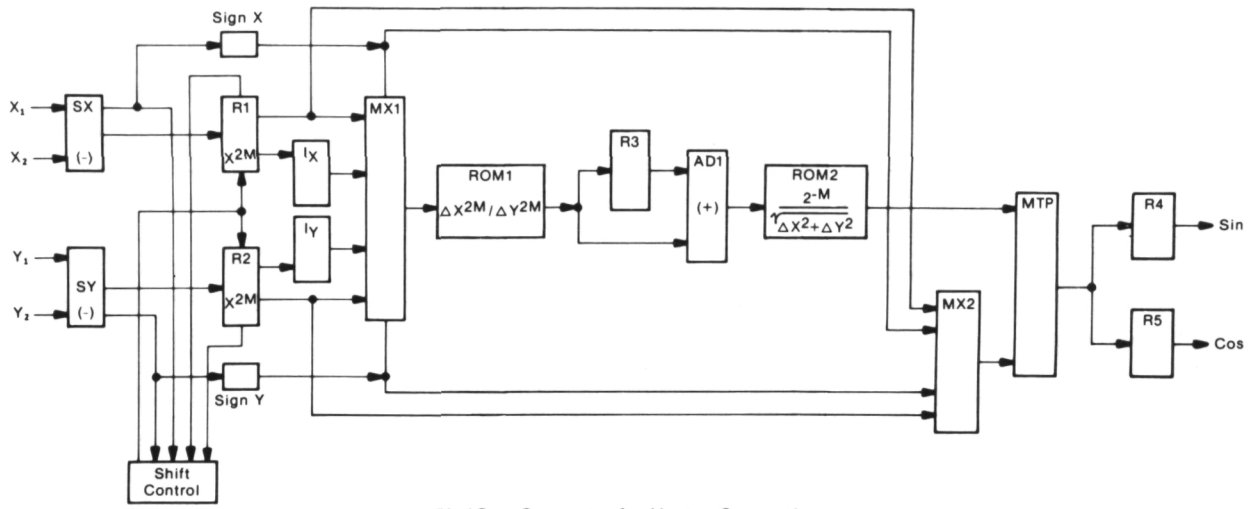
A variety of tapes and formats is available in a refresh memory. At some point during the refresh period, a tape format with an associated tape update value is transferred to a local memory. There the tape parameters are available for use by the tape-control routine. At that point the CRT beam is located at the left/bottom extreme of the tape baseline. This is the tape origin. The value at that point is the tape update value.

Tapes that require one or more format changes are stored as an equivalent number of parameter sets in the refresh memory. A link address specifies the location of the next format if required. This allows transfer between a variety of tape description parameters. The accumulated position is maintained, and the tape continues from the point of departure under the new data. The link address may specify the current tape format which results in a cyclic tape that wraps around on itself.

Source: R. C. Jones, S. V. Lazecki, and
R. J. Wetherel of
United Aircraft Corp.
under contract to
Johnson Space Center
(MSC-14545)

*Circle 2 on Reader Service Card.*

# SIN/COS COMPUTER FOR VECTOR GENERATOR




Sin/Cos Computer for Vector Generation

The generation of a stroke-written vector requires the derivation of the sine and cosine functions of a vector angle. A vector normally is defined by the coordinates of its end points: $X_1Y_1$ and $X_2Y_2$. In view of the use of read-only memories as lookup tables and the usually large range of values of $X_2$-$X_1$ and $Y_2$-$Y_1$, a special scaling or multiplication technique, to minimize the size of read-only memories, is used in the computer block diagram shown in the figure.

$X_2$-$X_1 = \Delta X$ is computed in SX, and $Y_2$-$Y_1 = \Delta Y$ is computed in SY. If $\Delta X$ and $\Delta Y$ are both below the maximum size for numbers permitted by the computer-word capacity, both are multiplied by a common factor, $2^M$, until the most significant bit of either word becomes a "1" or a "0", depending on the signs of both $\Delta X$ and $\Delta Y$. The shift control determines the value of M needed. The scaled differences are stored in registers $R_1$ and $R_2$. Circuit optimization can be accomplished by inverting all bits of negative scaled differences in $I_X$ and $I_Y$.

The multiplexer MX1 applies successive scaled values of $\Delta X^M$ and $\Delta Y^M$ to the read-only memory ROM1 that produces $\Delta X^{2M}$, which is stored in register R3, and $\Delta Y^{2M}$. These two quantities are added in arithmetic adder AD1, and the sum is applied to the read-only memory ROM2 that produces

$$2^{-M}/\sqrt{\Delta X^2+\Delta Y^2}.$$

The output of ROM2 is applied to the multiplier MTP as a multiplicand. The second multiplicand is switched by the multiplexer MX2.

In the first step of operation, the multiplexer MX2 selects $\Delta X^M$, and the output of the multiplier MTP is

$$\Delta X/\sqrt{\Delta X^2+\Delta Y^2}.$$

This quantity is stored in register R4 and represents the cosine of the vector angle. In the second step of operation, the multiplexer MX2 selects $\Delta Y^M$, and the output of the multiplier MTP is

$$\Delta Y/\sqrt{\Delta X^2+\Delta Y^2}.$$

This quantity is stored in register R4 and represents the sine of the vector angle.

This sin/cos computer should be of interest to those companies that manufacture digital processing equipment, and it may offer a convenient means for computation and the scaling of data.

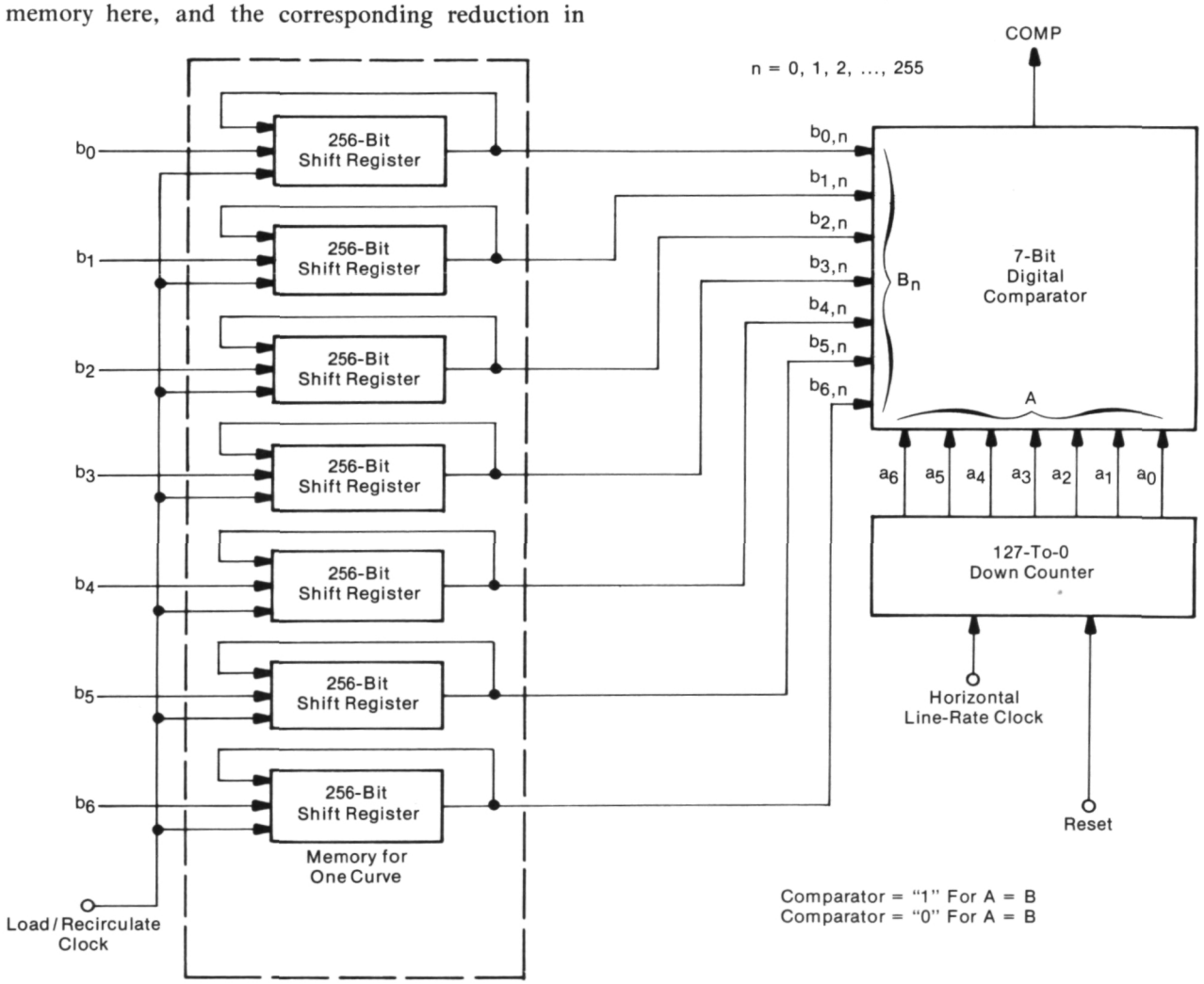
Source: S. V. Lazecki of
United Aircraft Corp.
under contract to
Johnson Space Center
(MSC-14543)

*Circle 3 on Reader Service Card.*

## DIGITAL CURVE PLOTTER

A curve plotter for a 525-line digital color television system has been developed. It can be used with scanned matrix displays and is capable of generating three simultaneous single-valued, multicolored curves. There are 256 data points, with a possible ordinate (amplitude) range of 128 discrete adjoining scan lines, available for each curve. The digital plotter (see figure) uses 5,376 bits of MOS shift-register memory to generate 3 curves with 7×256 bits per curve. Additional curves may be plotted by adding seven 256-bit shift registers and a 7-bit digital comparator for each curve. Similar plotters having full graphics capability require 256×128 (32,768) bits of random-access memory. The reduction in required memory here, and the corresponding reduction in overall circuit complexity, is made possible by using a binary algorithm based on single-valued curves.

The down counter (see figure) represents a 7×128 matrix. Each 7-element row of this matrix represents, in binary form, 1 of 128 discrete, scaled, ordinate values, corresponding to 128 interlaced field lines (256 frame lines for repeat-field video) centered in the visible television raster. The counter is organized so as to count down from the highest ordinate value to the lowest, at the horizontal line rate. For each curve, binary ordinate values are computed and scaled to correspond to each of 256 abscissa values. The ordinate values are then loaded into successive cells of a set of 256-bit shift registers.




Simplified Digital Curve Plotter

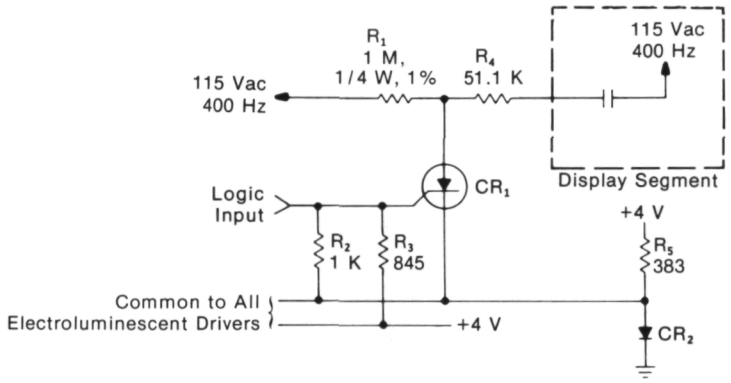
Each scan line is divided into 455 discrete adjacent intervals (140 ns per interval). A centered set of 256 intervals corresponds to the 256 data points per curve. The down counter and the shift registers are clock controlled so that each ordinate value presented by the down counter is compared in turn to each of the 256 abscissa values in the comparator. Thus, as each line is scanned, the contents of every shift register are recirculated in sychronism with the centered set of 256 data point intervals on that line. The comparator output (COMP), which is mixed with the digital video bit stream, is equal to 1 if the compared values are the same. It is equal to zero if they are not.

The contents of the plotter may be erased in less than 50 ns and rewritten in less than 300 $\mu$s. This allows display of rapidly changing curves. The scan lines are divided into 16 segments of 16 adjacent ordinate values each. Each of the three curves may take on one or more of eight available colors; but within a single segment each curve may have only a single color.

Source: J. K. Bergen of
General Electric Co.
under contract to
Johnson Space Center
(MSC-14095)

*Circle 4 on Reader Service Card.*

## ELECTROLUMINESCENT DISPLAY DRIVER CIRCUIT




Segment Driver Circuit

The illustrated solid-state driver circuit reduces the likelihood of malfunctions by eliminating the need for relays which have much higher failure rates than solid-state devices. Three improvements are afforded by this circuit: (1) increased reliability (life), (2) reduced power consumption, and (3) reduced size and weight.

The circuit is made possible by the development of a silicon-controlled switch ($CR_1$) that can conduct in both directions when an ac signal is applied. The circuit is triggered by a signal from the logic input, which is normally at +4 Vdc. This causes $CR_1$ to conduct and keeps the anode of $CR_1$ at approximately ground potential.

When the logic input signal switches from +4 V to zero, $CR_1$ is turned off, and 115 V rms at 400 Hz is applied to the electroluminescent display segment being driven, $R_3$ sets the base drive current. The purpose of $R_4$ is to limit the current in the event of a segment short. $R_2$ provides reserve bias on the base to prevent the turn-on of the electroluminescent display segment when the high voltage ac is applied and no logic power is present.

Source: C. B. Kirchen of
Grumman Aerospace Corp.
under contract to
Johnson Space Center
(MSC-12518)

*No further documentation is available.*

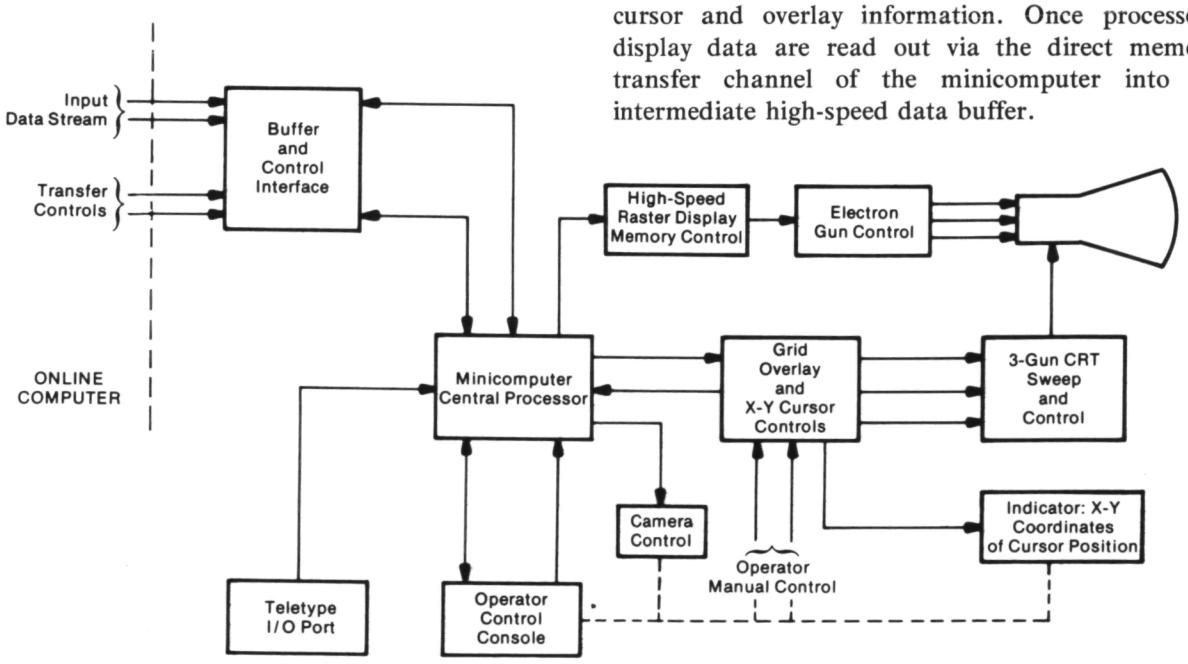
## COLOR-ENHANCED DATA DISPLAY SYSTEM

A general-purpose, programable data display system functions as a computer peripheral. The key feature of the system is the ability to provide color-coded enhancement of optical data. Detectors scan the object under observation and present the data to the main computer system which translates it into a color-coded image. This image, together with auxiliary data, is presented on a television monitor.

The display system configuration is outlined in the figure. All data processing is done under program control and is easily modified to provide custom display capabilities. Input data are received and processed by a large-scale computer system. Pertinent data elements are extracted, reformatted, and sent to the display unit in real time. The display unit incorporates a minicomputer to communicate with the main online computer, to read switch settings from a control panel, and to process and store the display raster data.

An interface logic panel performs the word length conversions necessary for communications between the two computers, and it contains line drivers and receivers to convert the input from the main computer logic levels to the TTL compatible levels used by the minicomputer. This panel also contains the cursor and overlay generating logic and the buffer storage and sync circuitry for the color television monitor. The minicomputer simulates the standard peripheral control signals required to communicate with the online computer.

As data is received, the minicomputer software converts the 14-bit, 8-bit, or 5-bit data values to 3-bit color codes. Color transformation is selected from among five stored color transformation curves. The color-coded raster is then stored in one of two buffer areas in the minicomputer, taking into account the scanning pattern of the detectors. One buffer area is then displayed while the other is being loaded, thereby giving a stable image. The display data are composed of three color signals and a sync signal. Two additional signals are presented to the monitor for cursor and overlay information. Once processed, display data are read out via the direct memory transfer channel of the minicomputer into an intermediate high-speed data buffer.




Display System Block Diagram

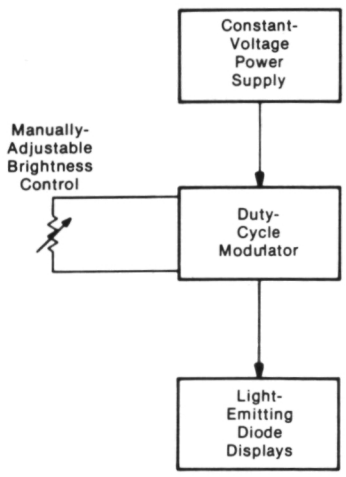
The minicomputer program also performs the necessary housekeeping functions. Included are procedures for detecting the start of raster sync in the incoming data stream, for displaying a raster count as color-coded elements of the display, for controlling a camera relay to photograph the displayed raster, for reading the control panel switches, and for controlling the status lamps and nixie tube readouts. The program operates under the control of a monitor which provides initialization of program parameters and recovery from erroneous data and which calls appropriate subroutines when necessary. The system program is loaded via a teletype paper tape reader and is read into the minicomputer over the serial teletype interface. The operator control console inputs and outputs are read in or out via digital input/output logic cards under control of the minicomputer program. The operator need only select the desired options.

Source: Systems Technology Associates, Inc.
under contract to
Goddard Space Flight Center
(GSC-11485)

*Circle 5 on Reader Service Card.*

## DISPLAY BRIGHTNESS CONTROL

The brightness control (see figure) for light-emitting diodes (LEDs) allows a display to be adjusted to a comfortable viewing level over a wide range of ambient lighting conditions. This is achieved by the duty-cycle modulation of the constant supply voltage at a repetition rate of approximately 100 Hz, which exceeds the response time of the human eye. A display appears brighter than the true average brightness when it is rapidly switched on and off. That is, a light that is rapidly turned on and off with a 50-percent duty cycle at full power appears to be brighter than if it were operated at 50-percent power.




Brightness Control Block Diagram

The brightness control has a manually-controlled duty-cycle range of approximately 0.7 to 70 percent, allowing the display to be easily seen with background light levels from darkness to ordinary room-illumination. The power supply can be made efficient because its output is a constant voltage. The duty-cycle modulator is also efficient because there is no power lost during the off portion of the cycle.

The control of brightness has previously been achieved by adjusting the supply voltage. This results in nonuniform brightness versus voltage relationship for individual displays. Another disadvantage is that power is lost in the voltage-regulating element which results in increased heating. The advantages of brightness control by duty-cycle modulation over that by voltage control include decreased power consumption and uniform brightness of displays at low-brightness levels.

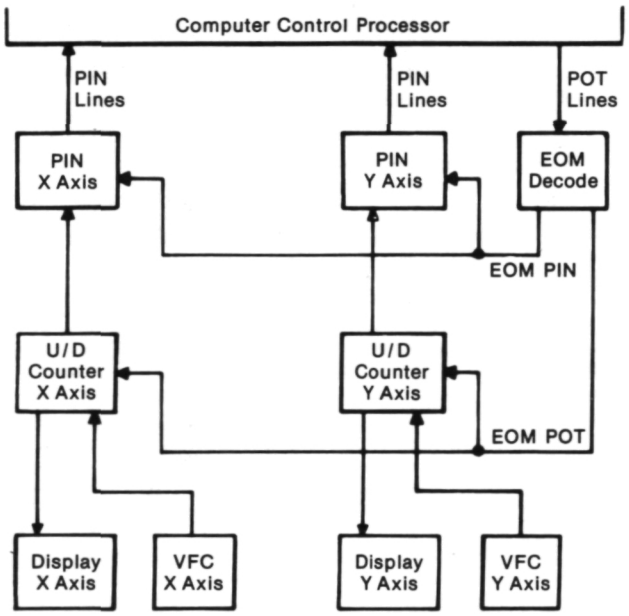
Source: D. G. Henies, G. L. Hornback,
and R. A. Wasylenko of
McDonnell Douglas Corp.
under contract to
Marshall Space Flight Center
(MFS-22965)

*Circle 6 on Reader Service Card.*

## NUMERICAL INTERACTIVE CONTROLLER

A controller has been developed to enlarge the picture displayed on a digital video display system. Any portion of the display can be viewed in an enlarged form for observation of specific details and features. It also includes a light-dot cursor for identification data cells on the enlarged display. The controller is a small, peripheral device, compatible with specific digital computers. It allows interaction of an operator with the data in the computer central processor in order to shift the frame of the data in Cartesian coordinates and slew the desired data into view. A cursor generator program is used in conjunction with the device to provide a light pen with sufficient resolving power to identify any particular set of coordinates with single-cell accuracy.

The numerical interactive controller (NIC), which generates pulses of variable repetition rates, clocks the X and Y axes. The variable clocking in the X and Y data registers, which are transferred to the computer, allows an image displayed on a digital video display system or an X-Y plotter to be displaced a corresponding amount in the X and Y directions. The amount of shift in each axis is conveniently monitored by a 3-decimal digit plus sign display, using positive and negative number cyclic counting. A lever on the device is used for coordinate control, which controls the frequency of pulses used for shifting the data. The greater the displacement from center, the higher the pulse rate; the direction of the displacement determines whether the numbers are increasing or decreasing in the X and Y registers.




The functional flow diagram illustrates the interface with the computer. The NIC is composed of two duplicate channels (X and Y), each comprising a variable frequency clock (VFC) oscillator and controller capable of generating pulses from 1 Hz to 1000 Hz in two ranges. The pulses from the VFC oscillator and controller are counted in an up/down (U/D) counter having a count display which shows the decimal count and the direction of counting. Counts cycle to 999 in the positive direction, change sign and then count from -998 to zero; the counting and display is cyclic. It is necessary only to keep track of the number of cycles in a large displacement; the three decimal digits in the positive and negative directions give high resolution with minimal hardware. The count in the up/down counter is strobed into a specific computer register (via parallel input PIN) and then into memory where data can be used to displace or otherwise enter into a computation. The NIC can be preset by the computer via parallel output (POT) so that the data is stored in the up/down counter and displayed on the 3-digit display.

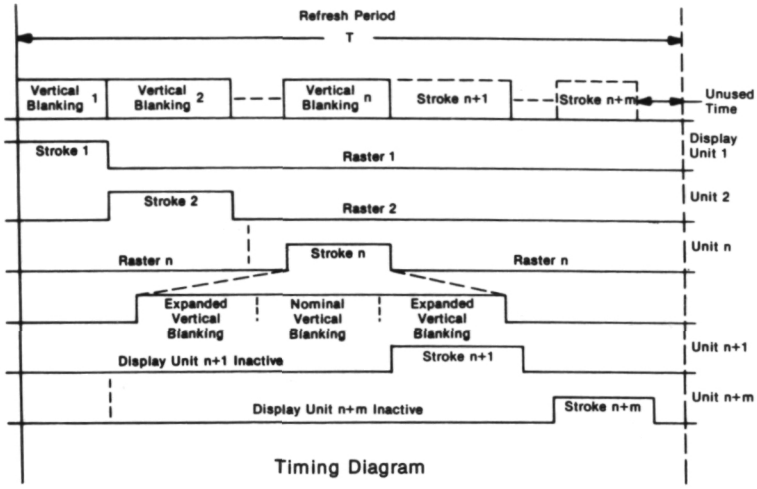
The energize output medium (EOM), PIN, and POT commands are timed signals. Parallel input/output operations, where a data transfer of up to 24 bits is involved, consists of two instructions. Before the transfer of data can occur, an EOM signal must be given to alert the NIC that an exchange is imminent. The instruction following the EOM will be either a POT for data leaving the computer, or a PIN, if the transfer is to be into the computer.

A digital video display system, with which the NIC can be used, is described in NASA Tech Brief B73-10132.

Source: Stanley S. Brokl and
Arthur I. Zygielbaum of
Caltech/JPL
under contract to
NASA Pasadena Office
(NPO-11497)

*Circle 7 on Reader Service Card.*

## PROGRAMABLE DISPLAY SYSTEM




Timing Diagram

A programable cathode ray tube (CRT) display system increases the capability of conventional systems and allows a wider variety of physical phenomena or simulations to be exhibited. The system has several key features:

a. Several stroke images are available from a single stroke generator;
b. Raster formats (lines/frame) are available for each of several display units;
c. The time available for stroke-write during vertical retrace is increased;
d. There is a flexible programable system for assigning raster and stroke images to multiple display units; and
e. An adaptive timing technique increases the efficiency of the allocation of stroke-write time.

The system has a single stroke-write generator and several raster generators. These are used with a number of display units which can contain independent images, each of which may be a combination of stroke-written symbology and raster format. A common refresh period is used for all the units. The time in the refresh period is partitioned as shown in the figure. The stroke-write generator writes on each unit during the vertical blanking period. These periods do not overlap. After stroke-writing is completed on the display units with rasters, stroke-written symbols are then generated on the remaining units.

The display content is limited by the portion of the refresh period allocated to stroke writing. To increase the time available, the vertical blanking is expanded and a word representing the number of raster lines of expansion is added to both sides of blanking, in half-line increments (to preserve symmetry). The number of expansion lines for each raster can be selected and programed into the system; a vertical rate counter provides the field/frame interval timing.

Digital timing circuitry is used to insure a common refresh rate and synchronous clocking for all the rasters. Rasters with the same number of lines are grouped together and blanked during the same period, allowing a single horizontal saw generator to be used with each group. The timing circuit also allows a portion of the horizontal rate counters to be shared by displays having rasters with different numbers of lines. This is accomplished by factoring the number of clock periods per line for the different rasters, and using a common counter for rasters with identical factors.

When the system is put into operation a preface program assigns a stroke-image starting address and a raster (with expansion lines) to each channel; and a display channel is assigned to each display unit. This gives the system enough flexibility to allow complex images to be put on multiple displays, by combining stroke and raster symbology.

Source: S. V. Lazecki and
R. J. Wetherel of
United Aircraft Corp.
under contract to
Johnson Space Center
(MSC-14544)

*Circle 8 on Reader Service Card.*

# A MAGNETICALLY FOCUSED IMAGE TUBE EMPLOYING AN OPAQUE PHOTOCATHODE

Optical images in infrared or ultraviolet spectra are beyond perception of the human eye. To see them, the observer normally uses an image converter that reproduces these spectra in visible light. This device converts ultraviolet and infrared optical images into electron beams which are projected on special screens making them visible. Unfortunately, existing image converters utilize relatively inefficient semitransparent photocathodes. These converters are difficult to manufacture, and their performance varies greatly from unit to unit.

An image converter has been developed which uses an opaque photocathode for improved efficiency. The device is easier to fabricate than the previous semitransparent photocathode converters and uses compounds from Groups III-V that are responsive to wavelengths between the ultraviolet (approximately 100 nm) and the near infrared region (approximately 1000 nm).

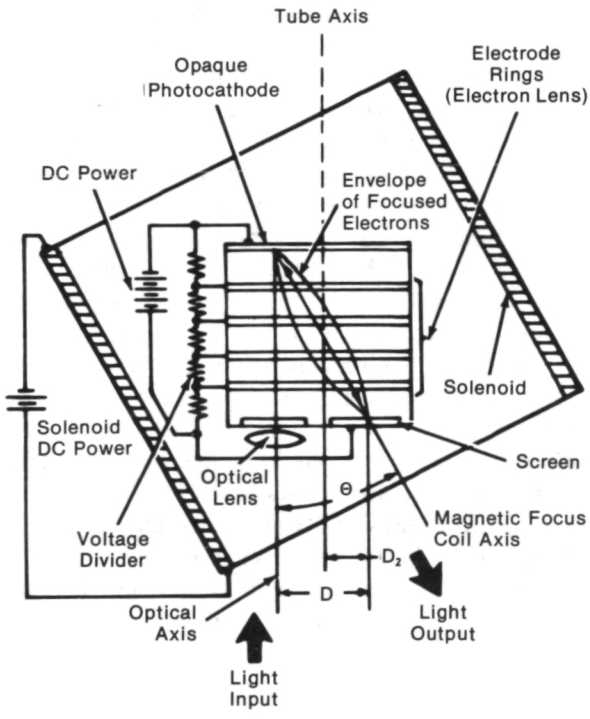



Image Converter

The image converter (see figure) is a vacuum tube which includes a flat, opaque photocathode electrode at one end and a flat electron target electrode (screen) at the other end. The screen may be a phosphor surface for a direct optical readout of the electron beam image derived from the photocathode or a gain/storage electrode read out by an electron beam. Both the electrode and the screen are within the line of sight of each other. Their planar faces are laterally displaced relative to each other so that an optical image on the emitting face is not obstructed by the screen. In response to the optical image focused on its surface, the photocathode emits an electron beam. This beam is then focused by the electron lens onto the phosphor screen.

The electron lens establishes a constant, dc, homogeneous electric field having a longitudinal vector along and parallel to the optical axis. It also provides a constant, dc, homogeneous magnetic field having a longitudinal vector between the photocathode and screen along and parallel to the magnetic focus coil axis. The magnetic coil axis is tilted at an angle Θ from the optical axis.

The constant, homogeneous electric field is established by several evenly spaced, parallel, annular, metal electrode rings on the inner circumferential wall of the tube. The dc power supply whose negative and positive terminals are, respectively, connected to the photoelectrode and the screen, also provides a different intermediate potential on each electrode ring at several points along the voltage divider. The voltage at each of these points is proportional to the distance of the particular electrode ring from the photocathode.

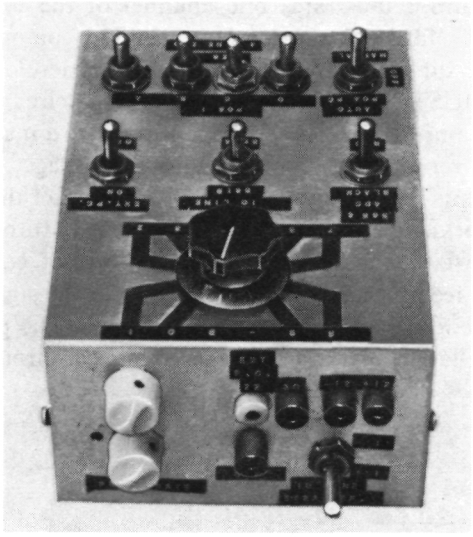
In operation, the image on the optical axis is focused by the optical lens onto the photocathode surface. The photocathode emits electrons that are accelerated by the homogeneous constant electric field and focused by the magnetic field produced by the

solenoid along the tilted axis. The electrons are uniformly accelerated along the tilted axis by the combined actions of the homogeneous, constant, electric and magnetic fields. The magnetic field also imparts cyclotron motion to focus the electrons on the screen. When the electrons strike the phosphor screen, they produce a visible image.

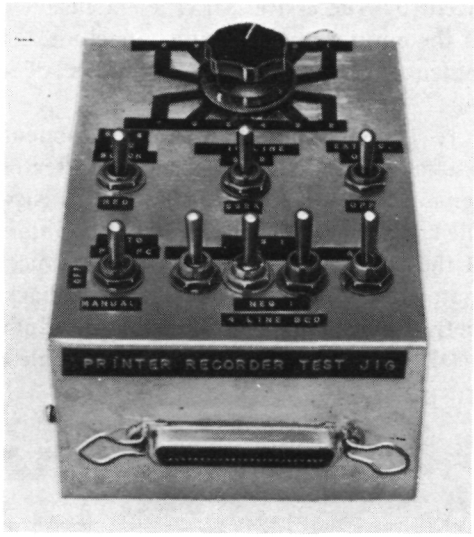
Source: C. Bruce Johnson and
Kenneth L. Hallam of
Bendix Corp.
under contract to
Goddard Space Flight Center
(GSC-11602)

*Circle 9 on Reader Service Card.*

## TEST ACCESSORY FOR PRINTER RECORDERS



Front




Rear

Test Accessory for Printer Recorders

Whenever a digital printer has to be repaired or checked out, one has to refer to the manufacturer's manual, and then make the necessary connections on specified terminals to set the printing wheels. A test accessory has been developed which provides the input for resetting these print wheels. The accessory includes several cables with plugs to match various printers.

The photograph shows the test set and the rear connectors that adapt the tester to four-line BCD units, including Clary 4000, ADC 3-9076, and the tenline Hewlett-Packard 561B and 562A models. The test set and cable are also adaptable to other printers. By selecting and connecting the appropriate cable, the printer can be set by dialing the number sequence. This makes checkout of a digital recorder-type printer quick and convenient.

Source: R. G. Knorr and L. T. Kieft of
Rockwell International Corp.
under contract to
Johnson Space Center
(MSC-17845)

*Circle 10 on Reader Service Card.*

## SIGNAL ACQUISITION FROM CHARGE-STORAGE-MODE PHOTOSENSOR ARRAYS

Many faults and anamalous effects attend conventional signal acquisition from large-scale charge-storage-mode photosensor arrays. In nearly every instance, such problems can be traced to an array-scanning arrangement which requires both signal commutation and signal acquisition to be accomplished directly at the array access terminals. Thus, arrays of phototransistors, which address their array elements by the cross-coincidence of orthogonal x-y access lines, are subject to parasitic effects that act to load or otherwise degrade the signal information produced by successive array elements. Of these effects the emitter bus shunting capacitance, $C_{ep}$, is preeminent in the loading operations of emitter readout.

Figure 1 shows the significant components of a single array element. In the case of emitter readout, the signal-developing load resistance, $R_L$, is switched into the emitter lead during its sampling interval. To negate the loading effects of shunt capacitance and to eliminate effectively the load-related feedback cross-talk between elements, a new technique, dump-and-store (DUST), capitalizes on the undesirable loading structure by introducing an externally-controlled forcing function at the emitter terminal to swamp the effect of $C_{ep}$. The DUST acquisition interface has been made practical by the application of a solid-state current transformer (Figure 2). This circuit, a 3-transistor network having an inherent input impedance on the order of 0.1 ohm, exhibits almost perfect linearity over an extreme range from nanoamperes to amperes when driven by either voltage or current sources, and it realizes very high transfer efficiencies (typically at least 99.999 percent).

Figure 2 illustrates one channel of the multiple-input, field-effect-transistor (FET) commutated, signal-summing circuitry that has been developed for the DUST system. The output of this circuit is an overdamped sinuoisdal voltage wave with a maximum value very nearly equal to the input voltage. Passive elements $R_f$ and $C_f$, included at the input of the $S^2CT$ network, act to roll off the signal throughput bandwidth and to dampen the effects of coupling-pulse feedthrough spikes coupled onto the signal line by the FET gate-to-source capacitances. The primary cancellation of these spikes is realized through the

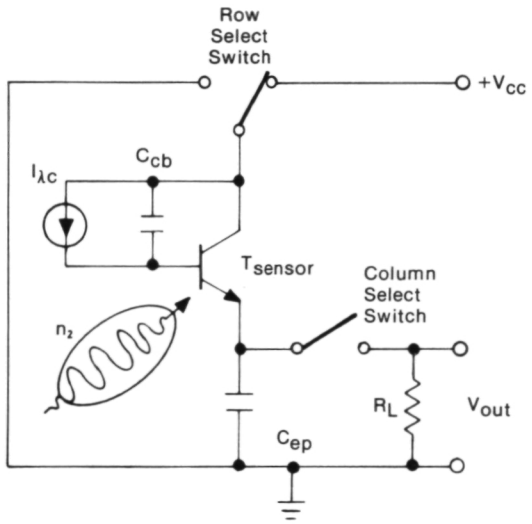



Figure 1. Signal-Acquisition, Single-Photosensor Array Element

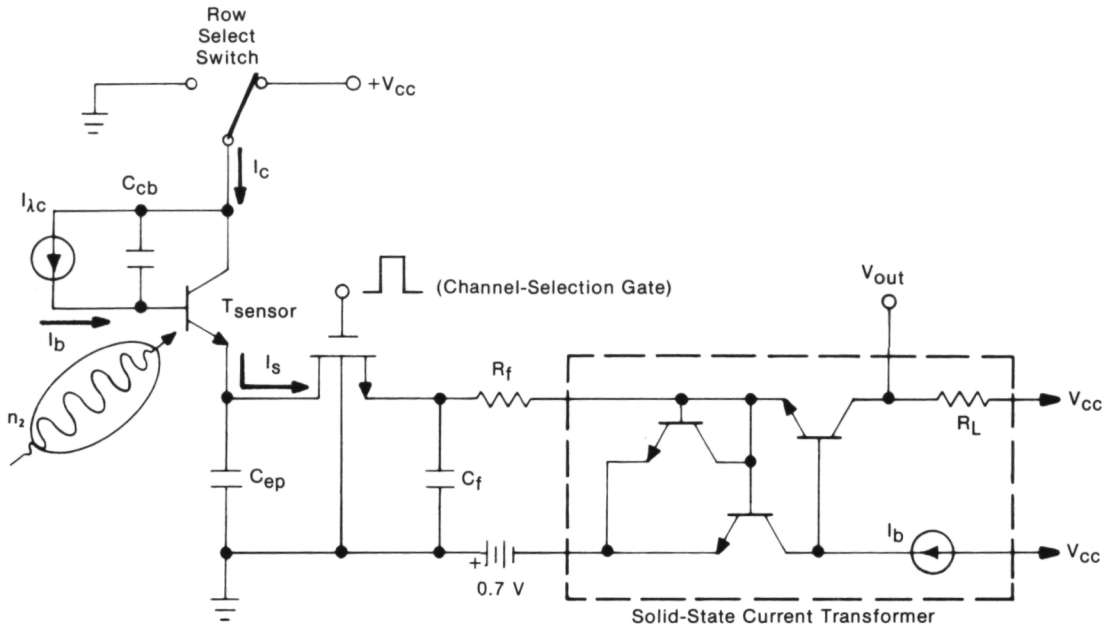



Figure 2. Typical Channel, FET Commutator

coincident selection and deactivation of adjacent channels. Signals as small as 1 mV have been successfully commutated at rates in excess of 2 MHz.

The sensor terminals are held at either supply or ground potentials at all points in the operating cycle and are not allowed to vary in response to the array output signals. All load-related feedback charge disturbances within the array are therefore completely eliminated. This results in a major reduction of inter-element crosstalk noise, leading to a significant improvement in the uniformity of the final output video and hence in image reproduction.

Elements in the array which are defective as a result of fabrication anomalies or crystallographic dislocations cause short circuits. The commutation of these elements produces a direct connection of the $V_{CC}$ supply to the output point, resulting in a very-high-amplitude video signal. Since dumping action begins simultaneously with the activation of the first array access line that is biased ON, and is completed within a very short interval thereafter (usually less than a microsecond), there is no need to maintain the bias voltage at the address terminal once the process is complete. Thus, the effect of the problem (bright spots on the display raster) can be negated by pulsing the drive voltage. Measurements taken with $S^2CT$-based DUST electronics on 50×50, 100×128, and 200×256 element phototransistor mosaics have revealed virtually unity gamma factors over more than 3 decades of incident irradiance.

Source: D. L. Farnsworth of
Westinghouse Electric Corp.
under contract to
Marshall Space Flight Center
(MFS-22629)

*Circle 11 on Reader Service Card.*

## VIDEO ENHANCEMENT OF X-RAY AND NEUTRON RADIOGRAPHS

Neutron and X-radiographs could be interpreted more easily and much more accurately if selected portions of the images were electronically enhanced and displayed on a viewing screen in real time. For this purpose a system has been developed for displaying radiographs on a television screen and enhancing the fine detail in the picture. The system uses analog-computer circuits for enhancing the contrast of fine lines and edges by processing the television signal from a low-noise television camera. The enhanced images are displayed in black and white on a television screen and can be controlled to vary the degree of enhancement and magnification of details in either radiographic transparencies or opaque photographs.

The first step in the process is to convert the original picture into a form suitable for electronic processing. This is accomplished with a video camera equipped with a lens system capable of viewing an area of 22.5×30 cm (9×12 in.) to an area as small as 0.95×1.27 cm (3/8×1/2 in.) as required. In the case of radiographic transparencies, the film is back illuminated with a self-contained cold light source. The camera converts the density values in the photograph to a television video signal. This signal is then processed to produce a new signal whose amplitude is proportional to the rate of change of density (i.e, the first derivative of density) across each raster scan line composing the video image. The enhanced image is displayed on a television screen. In this enhanced image, regions where there are changes in photographic density are accented in a manner that makes density variations stand out as though rendered in bas-relief. For example, points, lines, and edges that are seen only as subtle density differences in the original picture are brought out in sharp relief or contrast. Figure 1a is a neutron radiograph of an experimental tantalum-clad, uranium nitride fuel capsule with a barely-visible 3-mil-wide slot machined in the cladding. This slot plus other details are much

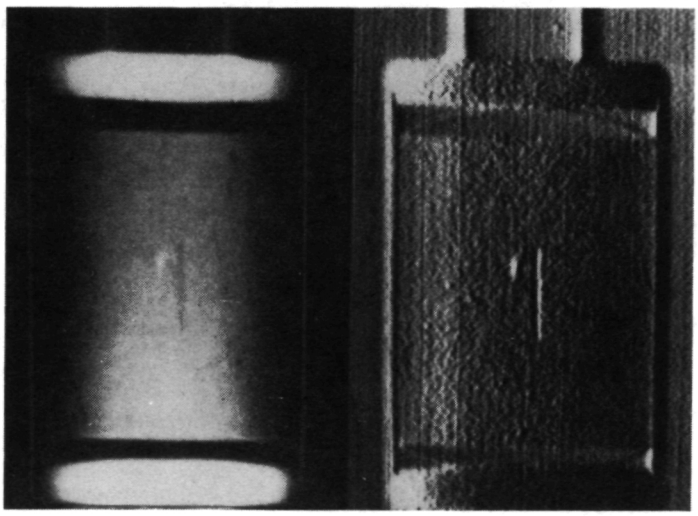



Figure 1. Enhancement of Radiograph of Experimental Nuclear Fuel Capsule

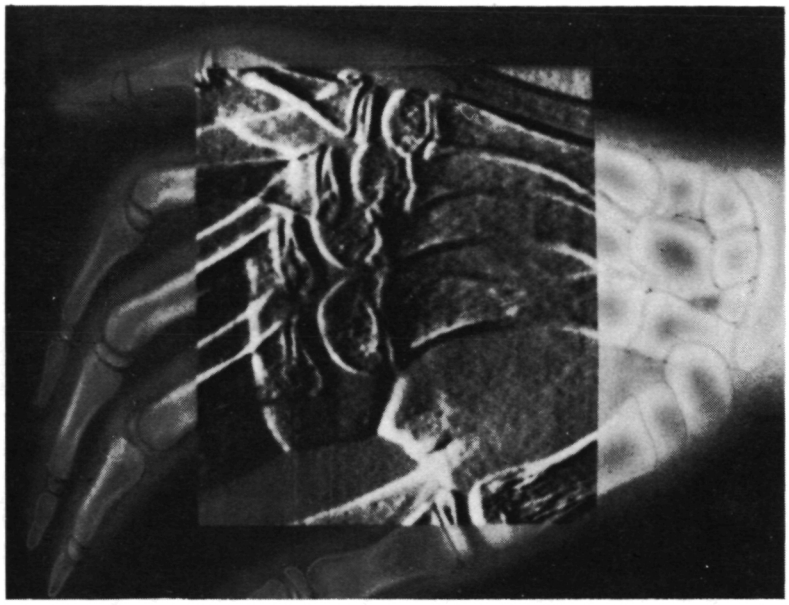


Figure 2. Radiograph of Human Hand With Center Portion of Radiograph Enhanced

more apparent in the video enhance, Figure 1b. Figure 2 is a medical X-ray as normally seen and an insert of the enhanced version. All the photographs were taken directly from the television screen.

The video enhancement system can be used to display pictures in the normal mode both as a positive or negative. In either the normal or enhanced mode, the contrast can be adjusted to reveal subtle density variations that might otherwise escape notice. Moreover, the image can be manipulated so that horizontal features are factored out in the enhanced version while vertical features only are accented. Or, the image may be set to bring out both horizontal and vertical elements in the enhancement. Another capability is to locate details with up to 30X magnification of images on the television screen in either the normal or enhanced mode.

This enhancement system has been applied to a variety of pictures including ordinary photographs, infrared photographs, metallographs, medical X-rays, and neutron radiographs of aerospace components. The system is a valuable adjunct to scanning microdensitometric image analysis. It can also be useful in nondestructive evaluation to complement other image analysis techniques (e.g., digital computer processing, photographic processing, and laser spatial filtering). An advanced version of the system combines black and white enhancement with a digital coded color television display.

Reference: More information on this image enhancement system is contained in the article entitled "Investigation of An Electronic Image Enhancer for Radiographs," Materials Evaluation - Journal of American Society for Non-Destructive Testing, December 1972, Vol. XXX, No. 12, pp. 259-267.

Source: Alex Vary
Lewis Research Center
(LEW-11944)

# Section 2. Signal Processing

## WIENER/KALMAN FILTERS

A classical Wiener filter is known to be an asymptotic version of a Kalman filter for a linear stationary system. Methods for obtaining a static filter (a Wiener filter) from the corresponding dynamic filter (a Kalman filter) have been developed for both the continuous and the discrete cases. In both cases a Wiener filter of a linear stationary system can be derived algebraically by finding eigenvectors of the eigenvalues associated with a matrix constructed from the coefficient matrices of error covarience (Riccati) equation. An analytical solution of a matrix Riccati equation of a general form has been previously discovered and developed, and similar techniques have recently been applied to solving the matrix Riccati equations arising in optimal control and prediction-smoothing problems.

An algorithmic relation between a Wiener filter and a Kalman filter of a linear stationary system, for the continuous case as well as the discrete case, has now been discovered. Eigenvalues with positive real parts for the continuous case (or those outside a unit circle around the origin of the complex plane for the discrete case), and the corresponding eigenvectors of a matrix associated with the linear system, are shown to be the only quantities needed to characterize the Wiener filter and the Kalman filter of the same linear system. The algorithm has the following properties:

a. The transient solution (a Kalman filter) of a matrix Riccati equation is presented by means of elements of the asymptotic solution (a Wiener filter),
b. The property of spectral factorization in the classical Wiener filter theory is shown to be inherited by the corresponding Kalman filter, and
c. The similarity of Kalman filters of continuous formulation and of discrete formulation is established.

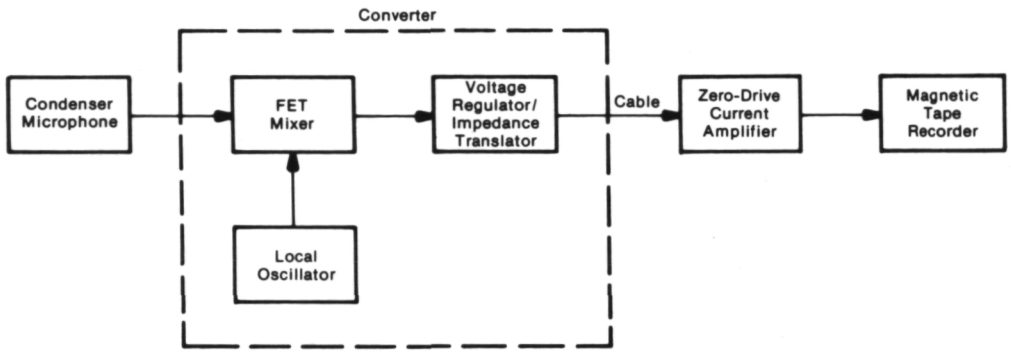
A Kalman filter is known to be asymptotically stable if the system is observable and controllable. The error covariance of a Kalman filter converges asymptotically to a constant matrix which is identical to the one obtained by the spectral factorization of the Weiner-Shannon theory.

Throughout the investigation, the observability and controllability conditions of the system are assumed to be satisfied. The algorithm has possible uses in the field of optimal control theory, for developing automatic controls, and in bioengineering and long-distance communications.

Source: Hiroshi Ohtakay of
Caltech/JPL
under contract to
NASA Pasadena Office
(NPO-11944)

*Circle 12 on Reader Service Card.*

## SOLID-STATE CONVERTER FOR MEASUREMENTS OF AIRCRAFT NOISE AND SONIC BOOM




Noise Measurement System

A new solid-state circuit produces an electric current that is proportional to the instantaneous sound pressure level at a condenser microphone. The invention, a carrier system, is designed to meet specifications with regard to noise floor, dynamic range, and frequency response, of such latitude as to render it suitable for the measurement of both aircraft noise and sonic boom.

Prior carrier systems are not well suited for aircraft noise measurements because of either high noise floor or insufficient high-frequency response. Those using a polarization voltage are unsuitable for sonic boom measurements because of insufficient low-frequency response. In general, such systems are sensitive to cable length and require impedance matching at the cable termination.

The figure shows a block diagram of the system in which the converter is incorporated. The converter produces an electric current proportional to the sound pressure level at the condenser microphone. The signal is transmitted over a cable, typically 548 m (1800 ft) in length, is amplified by a current amplifier, and is recorded on magnetic tape.

The converter consists of three stages (enclosed by the dashed box in the figure):

1. A local oscillator, which generates the carrier voltage applied to one of the gates of the FET;
2. A FET mixer, which uses a dual-gate FET to mix the microphone signal with the carrier, to produce an electrical current at the vibration frequency of the microphone diaphragm;
3. A voltage regulator/impedance translator, which regulates the voltage of the local oscillator and mixer stages, eliminates the carrier at the output, and provides a low output impedance at the cable terminals. The two circuits are combined into a single stage. The microphone cartridge and carrier electronics are integrated in the same physical package. This feature eliminates the need for the carrier to travel over the inter-connecting cable (as is the case in prior carrier systems) as well as associated problems, such as excessive capacitive loading of the microphone, crosstalk between adjacent units, and sensitivity of tuning to the cable length.

The zero-drive amplifier, although an external component, fulfills two basic functions essential to the operation of the converter. First, it serves as the power supply for all three stages of the converter; and second, in employing the recently-developed zero-drive principle, it terminates the cable in, essentially, a short circuit. This feature not only reduces the noise generated in the cable but also allows arbitrary lengths of cable, up to several thousand feet, to be used without impedance-matching networks.

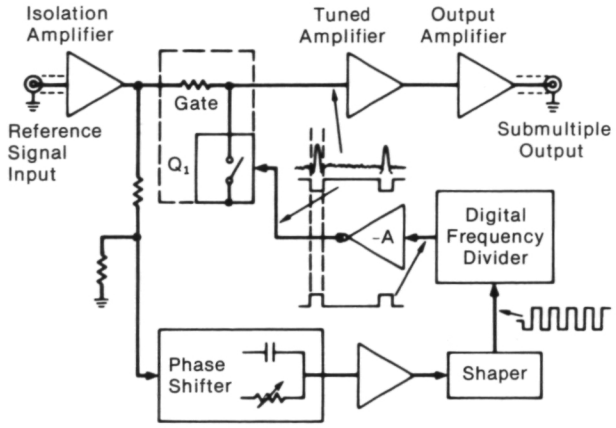
The following specifications have been realized in the prototype converter:

| | |
|---|---|
| a. Noise floor: | 52 dB equivalent sound pressure level. |
| b. Dynamic range: | 72 dB. |
| c. Frequency response: | dc to 28 kHz. |

Source: A. J. Zuckerwar of Youngstown State University under contract to Langley Research Center (LAR-11173)

*Circle 13 on Reader Service Card.*

## LOW PHASE-NOISE DIGITAL FREQUENCY DIVIDER




A new digital frequency divider system minimizes phase noise in the frequency-dividing circuits that are used in conjunction with atomic or maser frequency standards.

The system includes a digital divider and a gate which are used in such a manner as to avoid the noise which characteristically occurs in other types of dividers. A digitally-generated countdown pulse at the submiltiple frequency is applied to one electrode of an FET gate to establish a threshold state; the gate cannot function until the desired portion of the reference half-wave pulse which is to be passed appears on a second electrode.

As indicated in the diagram, a reference signal is introduced to the isolation amplifier and the amplified output is split; one portion is fed through a gate to a tuned amplifier, and the other portion is fed through a voltage divider to a phase-shift network.

The gate is essentially an FET transistor, $Q_1$, operated as a switch. When the gate electrodes of $Q_1$ are biased negatively, no current can flow between its source and drain and the device acts as a high impedance bypass on the output of the isolation amplifier; thus, signals coming from the amplifier pass to the tuned amplifier and thence to a broadband output amplifier. On the other hand, when the FET gate electrodes are biased positively, current can flow between source and drain, and the device presents a very low impedance to the output of the isolation amplifier, effectively short circuiting the output of ground.

The gate is controlled by an integrated circuit digital frequency divider set for any convenient division ratio which is a positive whole number. The fraction of the reference signal voltage coming from the phase shifter is amplified and then converted by a shaper into square waves of sufficient amplitude to drive the digital frequency divider module.

The output of the digital divider is a positive-going square wave, but since a negative-going keying signal is needed for operation of the gate, the digital frequency divider output is inverted by an amplifier at a voltage level sufficient to drive the FET gate transistor $Q_1$. Ordinarily, noise from the digital divider and the gate appears in the vicinity of turn-on or turn-off. When gating is effected as shown in the diagram, noise cannot pass into the tuned amplifier because the keying pulse from the digital frequency divider is kept at a level which does not permit gate-transistor $Q_1$ to open until the original reference signal positive half-wave crosses the zero axis in making the transition from negative to positive. During the interval defined by the negative-going portion of the keying square wave and the crossing of the zero axis by the reference signal, $Q_1$ remains in the conducting state, shorting the reference signal output from the isolation amplifier. The gate transistor goes into cutoff only when the negative-going keying pulse is present on the gate electrode and the positive-going portion of the reference signal appears on the drain; thus, transistor $Q_1$ is operated as an AND gate.

It is apparent that in passing through the various branches of the frequency dividing circuitry, the original signal will encounter different delays in each branch. The phase shifter establishes the time relationship between the particular cycle of the reference signal whose positive half-wave portion becomes the divided-down signal and the keying pulse at $Q_1$. A variable resistor in the phase-shifting network makes possible the proper coincidence of the reference signal and the keying signal.

Source: George F. Lutes of
Caltech/JPL
under contract to
NASA Pasadena Office
(NPO-11569)

*Circle 14 on Reader Service Card.*

## TIME-CODE DEMODULATOR SPEEDUP

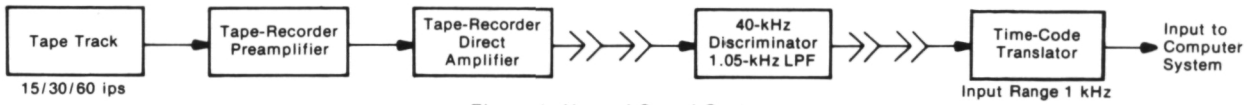



Figure 1. Normal-Speed System

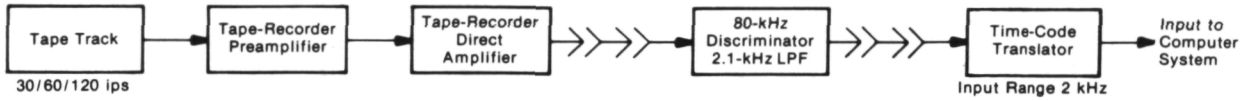



Figure 2. Double-Speed System

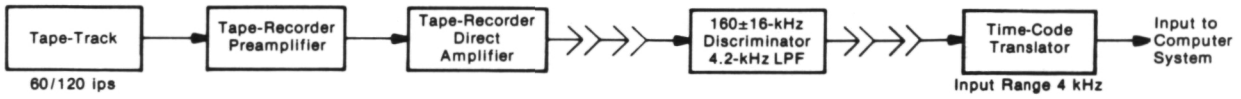



Figure 3. Quadruple-Speed System

A method has been developed to reduce the time required to process digital data previously recorded on magnetic tape. The reading speed of the tape is increased by a multiple of its normal speed, and the compressed signal is then fed through filter and data manipulation circuits to extract usable information.

With this technique, time-correlated pulse-code-modulated (PCM) signals, normally requiring 32 hours for processing, are processed in less than 12 hours. In the conventional processing system the time code recorded on magnetic tape modulates a 40-kHz voltage-controlled oscillator (VCO). The output of the VCO is frequency-division multiplexed with information from other VCO's and with the tape-speed reference frequency. The multiplexed signal is recorded on tape at 15, 30, or 60 inches per second (ips). The tape is then played back at the same speed at which the information was recorded, and the data is processed through a discriminator and a time-code translator (see Figure 1).

By replacing the standard discriminator with a higher frequency unit, the tape may be played back at a higher speed. Two systems have been used: one in which the playback speed is doubled (Figure 2), and one in which it is quadrupled (Figure 3). Thus the processing time may be reduced to one-half or one-fourth of real time.

In the system of Figure 2 the modulated time-code signal is patched to an 80-kHz discriminator, using a 2.1-kHz low-pass filter (LPF). In the system in Figure 3 the modulated time-code signal is patched to a 160)kHz constant bandwidth discriminator, using a 4.2-kHz low-pass filter. In both systems the data are then fed to a time-code translator, producing the timing signal input to a computerized data system.

Source: R. E. Mast of
Rockwell International Corp.
under contract to
Marshall Space Flight Center
(MFS-24239)

*Circle 15 on Reader Service Card.*

## HIGH SPEED DIRECT-BINARY TO BINARY-CODED-DECIMAL CONVERTER AND SCALER

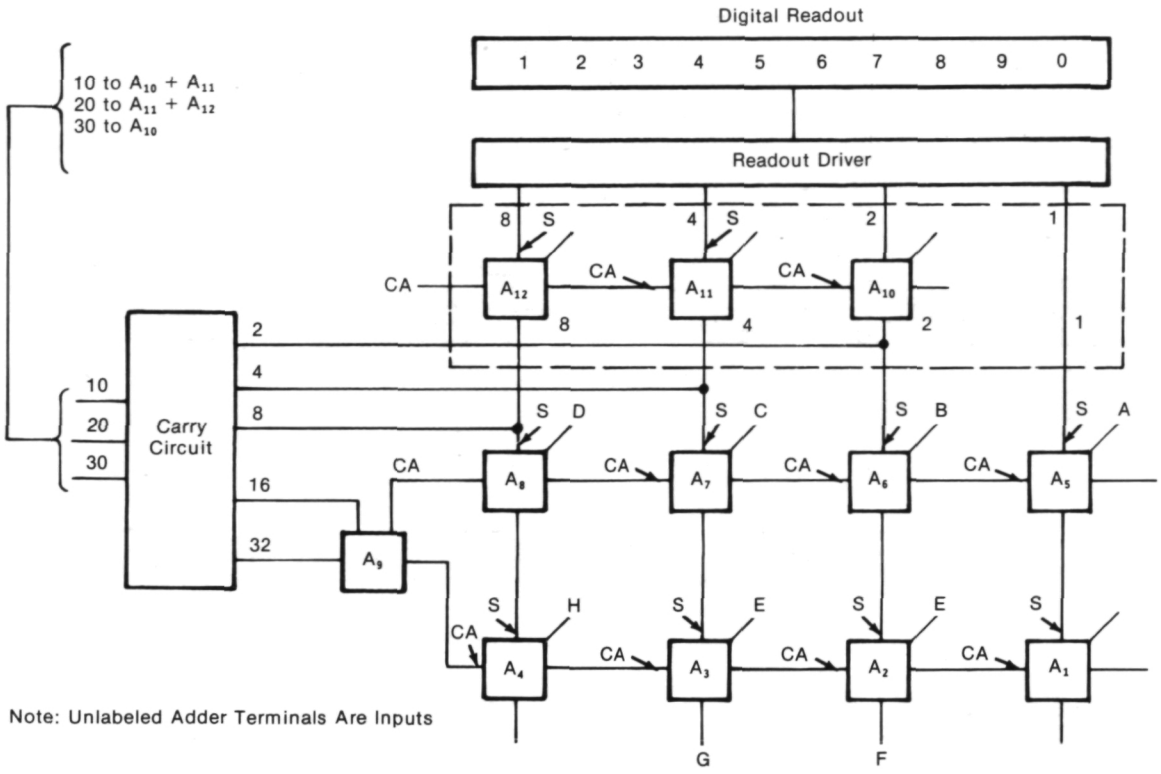



Figure 1. Units Readout Connected Adder Group

A telemetry (pulse code modulated) digital system, as a general rule, sends binary numbers representing some parameter that is not the value of the binary number. The received binary number must be scaled and converted to binary coded decimal to operate a readout device to display the true value. This conversion is usually accomplished by use of a digital clock and counter chain. The speed of the conversion has been limited by the speed of the clock pulses as well as the speed of operation of the counter and the associated hardware. The dependence of conversion on all these factors slows the entire data processing operation.

The clock and counter chain can be eliminated by a group of adders which speed up the binary number conversion and scaling in one operation. The group of adders that are used for this conversion are shown in Figure 1. The group shown is decade connected for producing units readout. Similar decades are provided for the 10's and 100's readout, etc. Each of the adders has three inputs, sum outputs (S's), and carry outputs (CA's).

The four adders in the bottom row have their carry output connected to an input of the next adder on the left. The carry output of adder $A_1$ is connected to input of adder $A_2$. The sum of output adder $A_1$ is connected to an input of adder $A_5$ in the row directly above. Similar connections are between adders $A_2$ and $A_6$, $A_3$ and $A_7$, and $A_4$ and $A_8$, respectively. The sum outputs of adders $A_6$ $A_7$, and $A_8$ are fed into a row of adders $A_{10}$, $A_{11}$, and $A_{12}$ which have their sum output connected to a readout driver. The driver is connected to a display tube which exhibits number "0" to "9".

In the conversion sequence (see Figure 2) the binary number is illustrated on the right, the decimal number in the middle, and reference characters A through H on the left. The latter represent the signals being fed into the adders. For example, if the binary coded number is 00000001, which is represented by character A, it will be fed into the readout tube and the numerical character 1 will be illuminated. However, if the binary character is 00010000, which is equal to 16, the character represented by E would be fed into adders $A_2$ and $A_3$. These adders would form

| Ref. Char. | Decimal Number | | | Binary Number |
|---|---|---|---|---|
| H | 1 | 2 | 8 | 10000000 |
| G | | 6 | 4 | 01000000 |
| F | | 3 | 2 | 00100000 |
| E | | 1 | 6 | 00010000 |
| D | | | 8 | 00001000 |
| C | | | 4 | 00000100 |
| B | | | 2 | 00000010 |
| A | | | 1 | 00000001 |

Figure 2. Conversion Sequence

the unit value 6 which is the units digit. The number 10 is carried into the next decade (not shown) and processed accordingly.

Scaling of the numbers is accomplished by the same circuit simultaneously with the conversion. Selection of the scaling factor is accomplished by use of different patchboard cards which are programed for each specific factor. These patchboards may be automatically controlled by using punch buttons.

Source: P. C. Toole
Kennedy Space Center
(KSC-10326)

*Circle 16 on Reader Service Card.*

## PHONOCARDIOGRAPHIC PREPROCESSOR: A REPORT

The final technical report on phonocardiographic preprocessors presents the results of a project intended to produce either a new circuit to extract heart-sound envelopes or an improvement to existing preprocessor circuits. Such a circuit is required to provide intensity (power) information and limited frequency data. The preprocessor should be portable, small, and include connections for a microphone or a recording unit. The output of the preprocessor is required to give the physician a pictorial representation of the heart sounds he hears. It should also provide a waveform that can be easily stored and analyzed by a computer.

A number of alternative solutions are presented. A breadboard circuit which extracts the envelope of the phonocardiogram is described. The circuit consists of a full-wave rectifier with simple resistance-capacitance filtering. The extracted envelope, however, has insufficient high frequency components and many of the characteristics of the phonocardiogram are not well defined. Appropriate filtering of the signal may solve these problems.

Source: Mohammad Ali Hooshmand and
Robert Martino of
George Washington University
under contract to
Goddard Space Flight Center
(GSC-11376)

*Circle 17 on Reader Service Card.*

## PHASE SHIFT KEYED, PULSE CODE MODULATED SIGNAL SYNCHRONIZER

Many data processing systems receive information impressed on an electromagnetic carrier (radio waves, for instance) in the form of pulses (pulse code modulation).

In one system the pulses represent a series of zeros and ones (bits) which contain data coded by shifting the phase of a given subcarrier [phase shift keyed (PSK)]. In cases where more than one subcarrier are used, the receiver may demodulate the higher subcarriers.

A PSK split-phase, pulse code modulated (PCM) signal is demodulated and synchronized by three loop circuits: (1) a "Q" loop that uses a quadrature signal to stabilize the frequency, (2) a "B" loop that acts on a baseband signal (a continuous frequency signal) to stabilize the phase, and (3) a decoding "I" loop, which acts on an in-phase signal. In a system in which the receiver output is a PSK split-phase signal, this synchronizer may be used to eliminate false-lock. False-lock occurs when the bit synchronizer bit-time differs from the incoming signal bit-time by 180° or 1/2 bit-time.

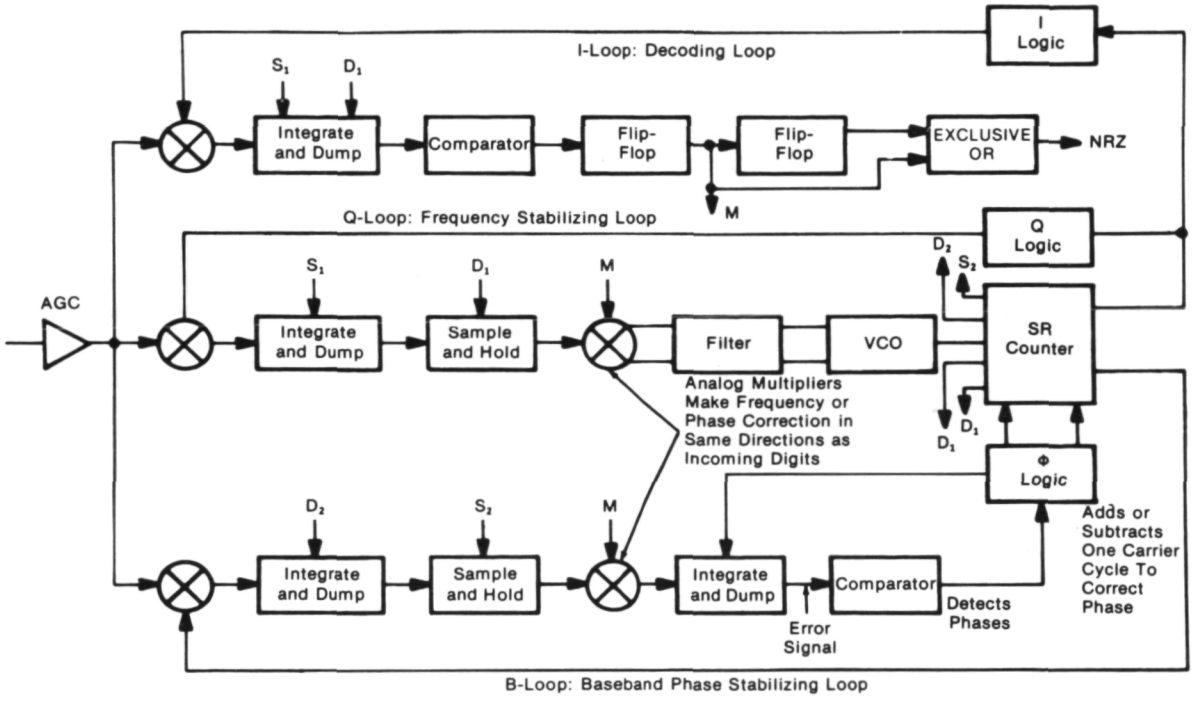



Diagram of Signal Synchronizer

The circuit is shown in the block diagram. The incoming signal goes to an automatic gain control (AGC) amplifier circuit. Here a power divider splits the signal into three parts, each going to one of the three loops, "I", "Q", and "B".

In the frequency-stabilizing "Q" loop, a voltage-controlled oscillator (VCO) provides pulses to a logic circuit. This circuit generates PCM signals with a 90° subcarrier phase shift, to be multiplied with the incoming signal. The product is integrated and sampled to detect error signals that are used to adjust the VCO signal until it matches the incoming frequency. This loop contains another multiplier (M) that receives its input from the "I" circuit. It changes the polarity of the error signals so that the correction for frequency is in the same direction for either an "0" or "1" value of the incoming bits. The "Q" and "I" will lock up on many null points depending on the subcarrier-to-data ratio.

In the "B" loop a continuous VCO signal is multiplied with the incoming signals. During each bit period the "B" loop signal is integrated and sampled at the end of each bit-time. The second integrator accumulates each bit-time error in the proper polarity as determined by the "I" loop data until the threshold value of the comparator is reached. The comparator output goes to the logic circuit which advances or retracts the relative phase of the generated frequency one subcarrier cycle at a time. The "B" loop shifts out of all subcarrier cycle nulls except the true lock null and the false lock null.

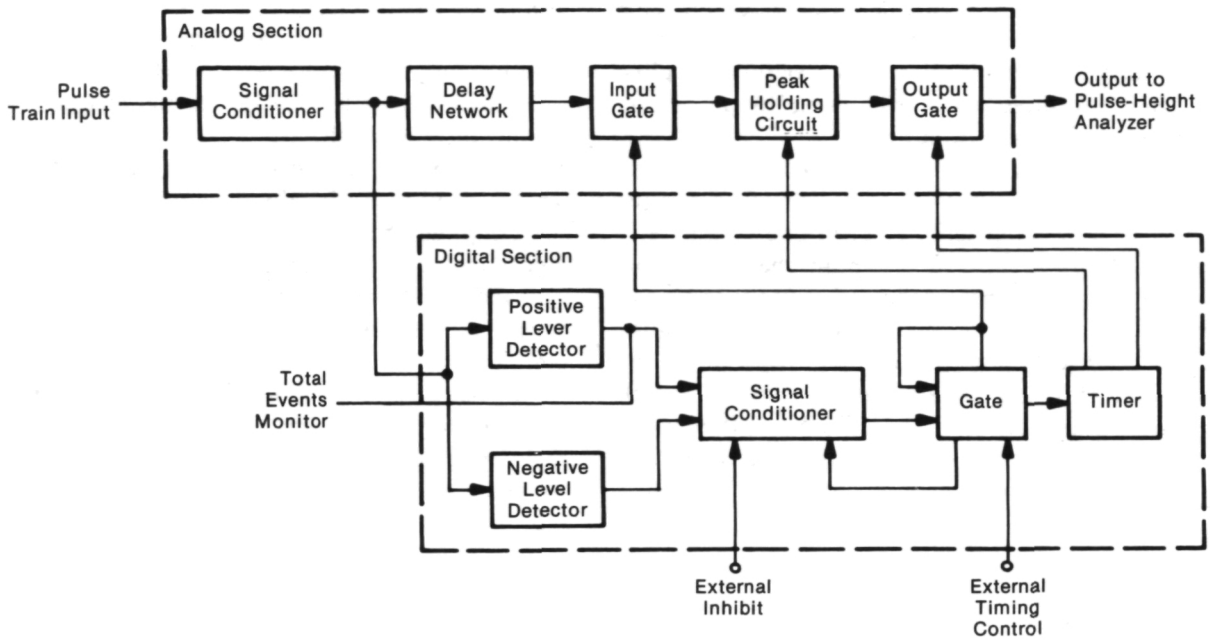
The "I" loop is the decoding loop. Here the I-logic signal is multiplied with the incoming signal. During the sampling period, the value of the bit is determined, and the comparator operates the flip-flops and the "exclusive or" circuit to provide a bit indication that is the circuit output to a de-commutator.

The false-lock in the PSK split-phase bit synchronizer is eliminated by the "Q" generated signal. The sensitivity or error signal is minimum for false-lock null while the error signal is maximum for the true lock null. By setting the "Q" loop sensitivity such that it will not lock on the minimum false-lock null, the bit synchronizer will always lock on the true-lock null.

Source: Herbert S. Kobayashi
Johnson Space Center
(MSC-12462)

*Circle 18 on Reader Service Card.*

## PULSE STRETCHER FOR NARROW PULSES




Pulse Stretcher

Present pulse height analyzers are not capable of processing pulses that are much narrower than 1 microsecond. For this they usually require a pulse stretching circuit which will extend these pulses to an acceptable width before they are fed into the analyzer input. Unfortunately, existing pulse stretching circuits have several drawbacks when used with narrow pulse widths. First, their output is nonlinear for narrow input pulses. This nonlinearity affects analysis of spectra for even low event rates. Second, they offer insufficient protection against pulse pile-up because of low rejecting analog gates located in the input circuitry. Third, they exhibit baseline distortion because of capacitive coupling of the unipolar or nonsymmetrical bipolar input signals. Fourth, they provide insufficient means of detecting the true number of input events for deadtime corrections.

A pulse stretching circuit was developed which can linearly stretch pulses as narrow as 50 nanoseconds and block incoming pulses following an accepted input pulse until processing has been completed. It also removes baseline distortion by being completely direct coupled and provides a monitor output which measures the true number of input events that exceed a predetermined threshold.

The pulse stretcher (see figure) is comprised of two sections: an analog or linear section, and a digital or a decision-making section. The analog section delays the incoming pulse with the delay network to allow the digital section to decide upon the disposition of the pulse event.

If the decision is to process this event, the input gate connected to the output of the delay network is opened and the pulse peak is detected and held for a selectable time interval by the peak-holding circuit. The holding circuit changes the narrow bipolar pulses to unipolar pulses which can be handled without distortion by the pulse height analyzer. The duration of the unipolar signal is determined by a dump command signal from the digital section.

Meanwhile, the digital section through logic commands prevents the succeeding pulses from changing the detected peak amplitude during the hold cycle. The undelayed analog pulse is fed to the digital section through two level detectors feeding a signal conditioner. The conditioned signal is fed to a gate with timing externally controlled. When the gate is opened, its output starts the timer which provides the dump signal for the holding circuit in the analog section to produce an output pulse having an amplitude directly proportional to the pulse peak height, but whose pulse shape is compatible with ordinary pulse height analyzers. The output signal has a positive polarity, and its baseline is at zero volts. The digital section control line to the input gate also inhibits any other input signals from being processed during a predetermined time interval.

The digital section then resets the analog section to process a new event and opens the analog input gate, provided a new pulse has not yet been received. If a new pulse is present, its processing is specifically inhibited, since its peak might have already passed and processing would result in an incorrect observation. The digital section guarantees the processing of one and only one analog pulse at a time by keeping the two analog gates closed, except when:

1. The incoming analog pulse has sufficient amplitude to trigger the negative level detector;
2. A minimum period of time has elapsed since the processing of a preceding pulse; and
3. A high level input signal is provided at the external timing control input or this input is left open.

Source: R. S. Lindsey, Jr., of
Lockheed Electronics Company
under contract to
Johnson Space Center
(MSC-14130)

*Circle 19 on Reader Service Card.*

## RF-TO-DIGITAL CONVERTER

Some automatic spectrum analyzers require a digital representation of an RF signal level. However, the RF-to-digital converters currently used with spectrum analyzers are expensive and complex. A new RF-to-digital converter can be used for automatic spectrum analysis. An automatic gain amplifier digitizes the RF amplitude, and the amplifier gain is measured by a binary counter. The amount of gain corresponds to the signal level and is proportional to the count in the counter.

A block diagram of the converter is shown in Figure 1. The RF input signal is fed through the amplifier; it is then rectified and fed to an RF threshold detector that produces an output-level command. This command controls the up/down counter. The gain of the amplifier is adjusted up or down to maintain a constant output signal.

The amplifier gain is calibrated in decibels. The actual count on the binary counter is therefore an indication of the gain of the amplifier in decibels,

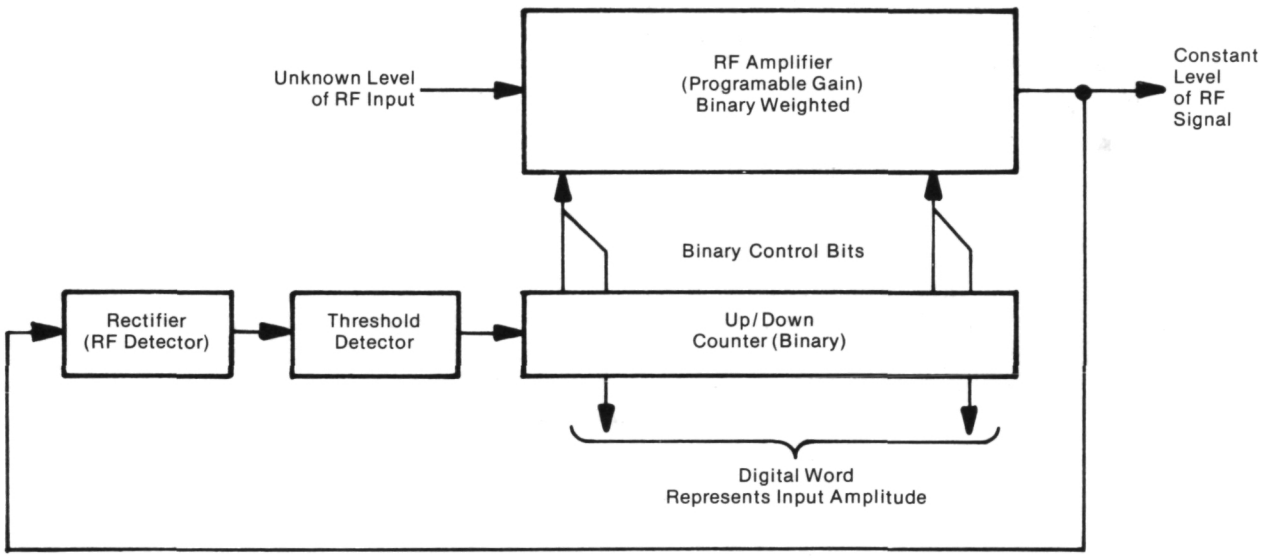



Figure 1. RF-to-Digital Converter

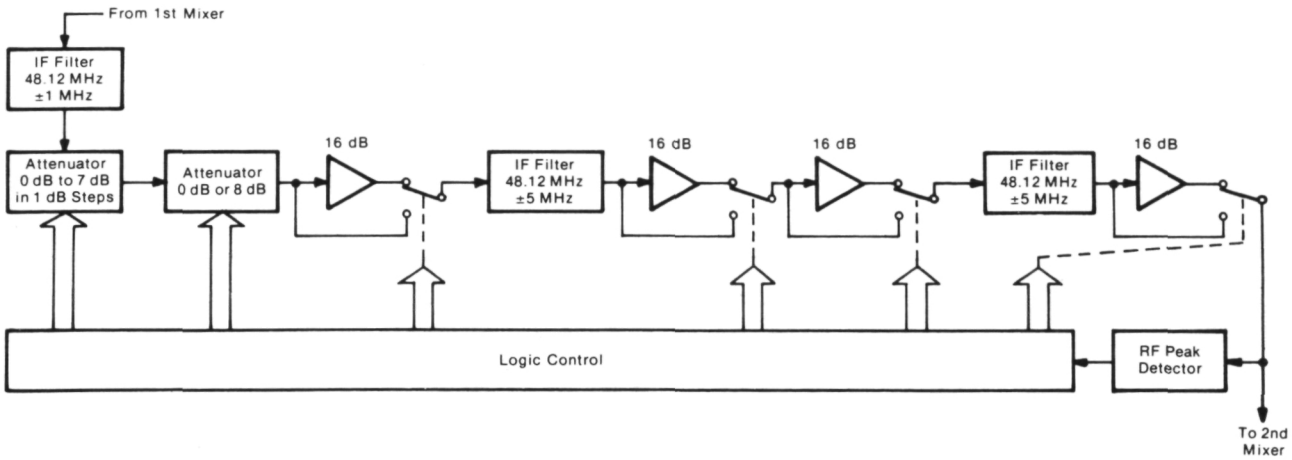



Figure 2. Automatic Gain Amplifier (48 MHz)

which is equal to the amplitude of the RF input with reference to the threshold detector.

Figure 2 is a block diagram of the amplifier. Solid-state switches control the RF level in 1 dB increments. Each of the four amplifiers can be independently switched in or out. For instance, one amplifier is used for a less than 16 dB gain, two up to 32 dB, etc.

The converter can measure RF signals from 50 MHz to 1.3 GHz; resolution is 1 Hz and accuracy to within 10 Hz. It can handle a minimum frequency spacing of 10 Hz, a maximum relative amplitude of 10 Hz, and has an amplitude range of +67 to -100 dBm.

This system can be used to calculate AM and FM modulation index, distortion of AM waves and pulse width and other parameters of pulse-modulated FM waves. It can be used in RF interference surveillance and automatic RF components tests.

Source: T. E. Flanders and G. Kosa of
General Electric Co.
under contract to
Johnson Space Center
(MSC-14419)

*No further documentation is available.*

# Section 3. Memory Systems

## AN IMPROVED HOLOGRAPHIC RECORDING MEDIUM

Thermoplastics have been considered as a recording medium for holographic optical memory systems. However, the thermoplastic materials that have been considered to date gradually fatigue and degrade. After repeated write-erase cycles, sharp, clear holograms can no longer be stored on the thermoplastic surface.

It has recently been discovered that solid, linear chain hydrocarbons with molecular weights ranging from about 300 to 2000 can serve as long-lived recording mediums in an optical memory system. Suitable recording hydrocarbons include microcrystalline waxes and low molecular weight polymers of ethylene. These hydrocarbons are unbranched, unsaturated, and have no active end groups. Why these polymers work so well is not completely understood, but it is believed that their long recording life is the result of the straight chain molecules not cross-linking on repeated heating and cooling.

A standard recording medium consisting of three layers is used: on the bottom a conductive substrate; in the middle, a photoconductive layer; and a deformable thermoplastic layer on the top. To record an image, a corona discharge device ionizes the air near the surface of the thermoplastic. The ionized air causes positive ions to be deposited on the surface of the thermoplastic. Next, this surface is exposed to an image carried by the coherent light from the laser object and reference beams. This light interacts with the photoconductor layer to redistribute the charges on the thermoplastic.

The thermoplastic is charged again, and the electric field increases in the previously illuminated areas. Finally, the wax is heated until it becomes softened (the characteristic property of thermoplastic materials), and the charges on the wax cause the formation of hills and valleys that are retained upon cooling. The medium is erased by heating (in the absence of the coherent light) until the information-carrying shape flattens out.

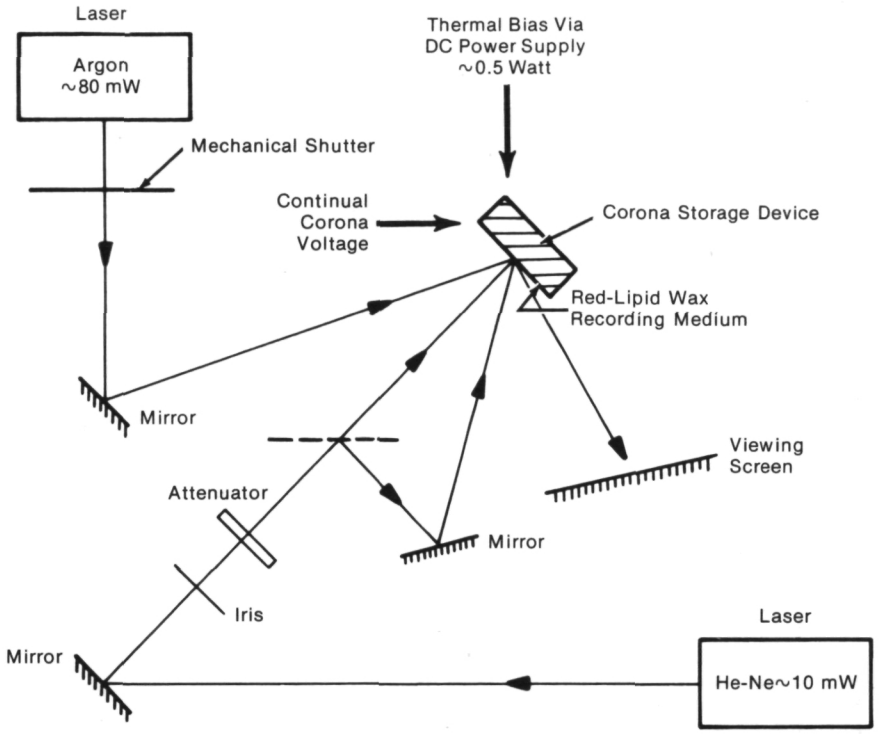
Several different materials can be used in the system, but a typical example will illustrate the principles. The conductive substrate is preferably a transparent material such as glass with a thin coat of indium or other conductor. The substrate is dipped into a solution of photoconductor to deposit a 1- to 2-micron layer. The photoconductor may be inorganic or it may be an organic material such as poly-N-vinylcarbazole. Next, the coated material is dipped into another solution, this one containing the thermoplastic material. The thermoplastic (for example, a linear homopolymer of ethlyene) should be from 3 to 7 microns thick. Recording media prepared in this way have been tested with 7000 write-erase cycles with no signs of fatigue.

To allow faster thermal softening, the deformable polymer may be heat biased. In this case the polymer is kept at a temperature just short of its softening point, so that it may be softened by raising its temperature only a few degrees. When this is done, it is desirable to include a fourth layer: an "insulating barrier", between the thermoplastic and the photoconductor. A thin layer of a highly polar, transparent, acrylic resin has been used for this purpose.

Source: R. A. Gange of
RCA Corp.
under contract to
Marshall Space Flight Center
(MFS-22532)

*Circle 20 on Reader Service Card.*

## LASER ADDRESSED HOLOGRAPHIC MEMORY SYSTEM




Microcrystaline Wax, Laser Storage System

A new holographic recall and storage system uses a red-lipid microcrystalline wax as the storage medium. The wax serves as an appropriate write/erase medium because it has, for waxes, a sharp, thermal crystal/plastic transition range (around 2° C).

The experimental arrangement is shown in the figure. The storage device consists of a TIC-coated glass substrate, a PVK photoconductor, an elevacite barrier, and the microcrystalline wax. A corona discharge ionizes the air around the wax causing it to become charged with positive ions. The holograph beam redistributes the charge. When the wax is softened, this charge causes thickness variations in the wax surface, representing the intensity pattern of the beam.

The wax is thermally biased (heated to a temperature just below the transition temperature) by direct current passed through the transparent TIC substrate. When the laser beam strikes the wax, its energy heats the point of incidence enough to pass the wax through the transition temperature. A holograph image can then be written or erased in the softened wax.

An argon laser at 80 mW provides thermal energy, and a helium-neon laser provides the second beam for the interference pattern. The resultant image may be read off a viewing screen.

Page selection is accomplished by moving the storage device. In a more advanced system, a single laser and an electronic light-modulator could be used to select pages.

Source: R. A. Gange, E. M. Nagle,
and C. C. Steinmetz of
RCA Corp.
under contract to
Marshall Space Flight Center
(MFS-22565)

*Circle 21 on Reader Service Card.*

## LASER-ACTUATED HOLOGRAPHIC STORAGE DEVICE

The automatic selection of one out of thousands of pages in a holographic memory system is a formidable task. The attempts that have been made to fabricate high-vacuum tubes which would use photoemitted electrons, to selectively heat desired holographic locations, have failed because of cesium contamination of the storage device.

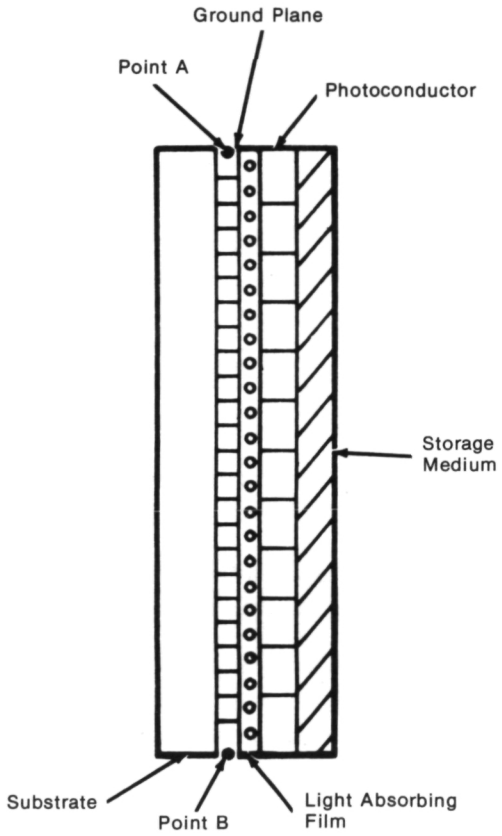



Figure 1. Laser-Actuated Storage Device

A new laser-actuated storage device permits the automatic selection of holographic pages by using a laser beam. The operation of the laser-actuated storage device is as follows. Constant power is applied to the conducting ground plane through a dc current between points A and B (see Figure 1). A uniform charge distribution is maintained over a useful portion of the storage medium through a corona-discharge chamber. In the presence of the uniform and continuous corona-discharge stream, the constant power bias is of sufficient magnitude to maintain the laser-actuated holographic storage device, at a temperature just below the thermal threshold of the storage medium.

The laser beam then is addressed to the desired location; absorption of the beam by the light-absorbing film increases the temperature locally at the desired holographic page address. The additional temperature increment causes the temperature to increase beyond the threshold of the storage medium; and a hologram is either written or erased, depending upon the specifics of a laser-beam modulation (see Figure 2). For example, if a deformable media such as microcrystalline wax is used, then the bias temperature $T_O$ would be as shown. In the figure, the temperature $T_O$ lies just below the temperature beyond which an abrupt change in viscosity occurs. It is desirable to bias thermally the laser-actuated device as close as possible to the "knee" of the viscosity-versus-temperature curve. In this manner, the temperature change ($\Delta T$) necessary to effect an adequate viscosity reduction during the writing or erasing of a hologram, is held to a minimum. Since the laser beam supplies the energy requisite to the temperature change, a small temperature change means less energy is required from the laser.

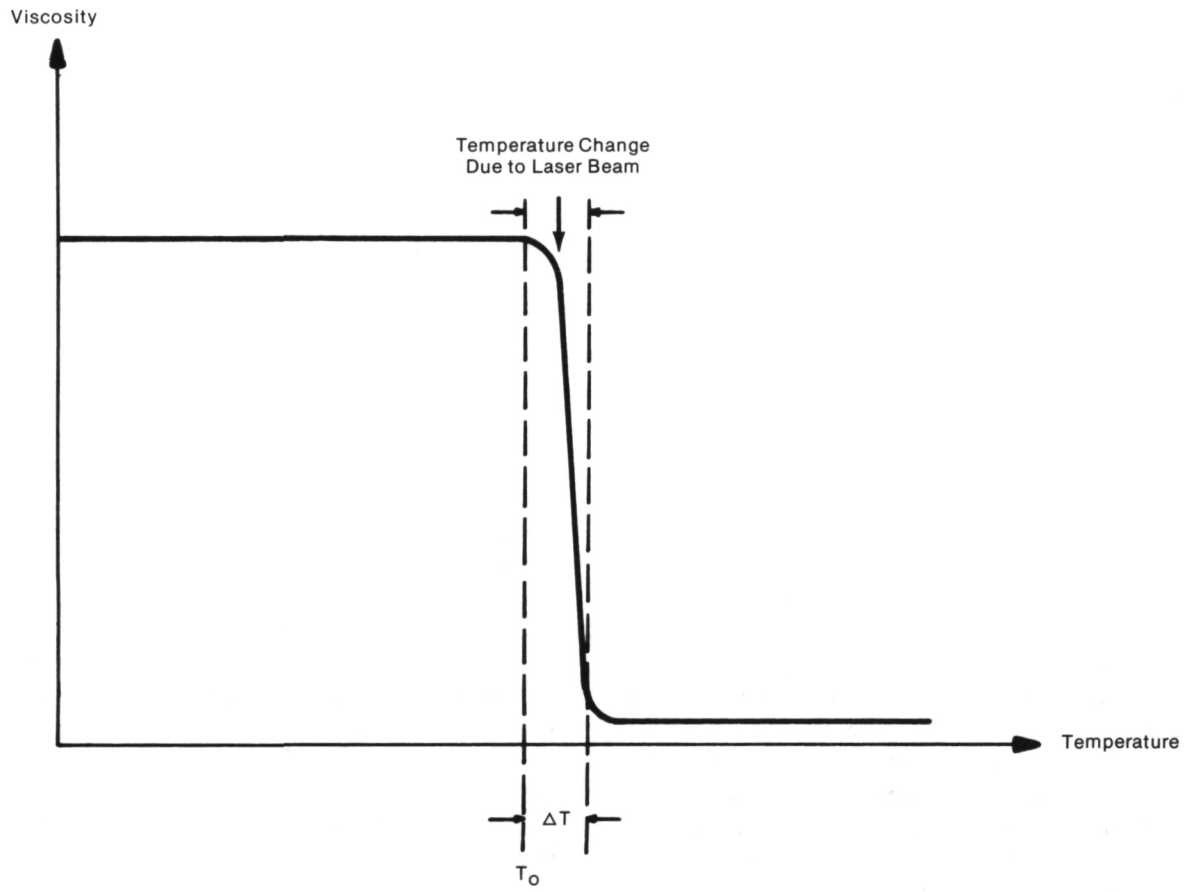


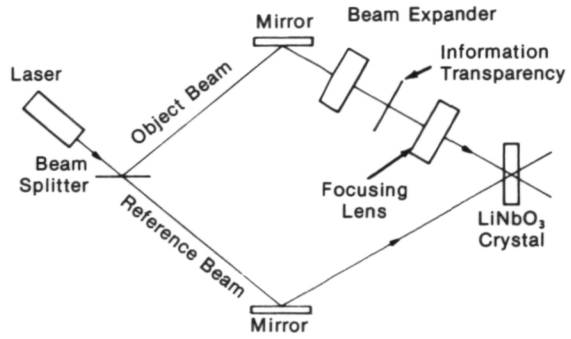

Figure 2. Viscosity as a Function Temperature (Storage Medium)

In a typical operation for a 2° to 3° C temperature interval, using a dc power supply with no power regulation, holograms were successfully written and erased over a 2-cm by 2-cm area, using an 80-mW argon laser beam. In this instance, glyptal was used as the light-absorbing film on the exterior side of the (glass) substrate.

Source: R. A. Gange, E. M. Nagle, and C. C. Steinmetz of RCA Corp. under contract to Marshall Space Flight Center (MFS-22768)

*Circle 22 on Reader Service Card.*

## A NEW OPTICAL RECORDING MEDIUM




BLOCK DIAGRAM OF HOLOGRAPH arrangement used to record information in single crystal $LiNbO_3$. Readout is accomplished by blocking off the object beam and illuminating the hologram with the reference beam.

One of the next advances in computer capabilities, a step which has been just out of reach, is the development of an erasable, optical-recording material for computer memories. Such a development would permit the rapid, inexpensive storage and recall of entire pictures as a single unit. It would permit the analog storage of TV frames, printed pages, photographs and other visual information that must currently be stored as a sequence of ones and zeros.

Several optical storage candidates have been under consideration for some time. Among these is a lithiumrare earth crystal, lithium niobiate ($LiNbO_3$). Crystals of $LiNbO_3$ have several favorable properties for use as an optical recording medium. They have a high information capacity, a high readout efficiency, and are erasable. In addition, they require no chemical developing and can be used to store three-dimensional holograms. However, $LiNbO_3$ has one severe drawback; it is not sensitive enough to record at the rate required in computer processing.

For a time it had seemed as though work on a suitable optical recording medium had come to a standstill. Thin films, thermoplastics, and other alternatives to $LiNbO_3$ all had inherent limitations offering little hope for improvement. But it has recently been discovered that $LiNbO_3$ crystals can record data at a much higher rate when doped with transition metals.

If an $LiNbO_3$ crystal is doped during growth with a transition metal such as iron, copper, or manganese, the optical properties are significantly enhanced, and the crystal becomes a highly promising optical recording medium.

The crystals are doped with from 0.01 to 0.5 weight-percent of transition metal. After growth, they are annealed, X-ray mounted, and sliced into 20×20 mm wafers one mm thick. Iron seems to be the best dopant. Iron-doped crystals will store a hologram image in as little as seven milliseconds using a commercial argon laser.

The recording process in $LiNbO_3$ is based on the electro-optic properties of the crystal. During crystal growth, the transition metal ions alter the optical absorption, electron concentrations, and trapping center concentrations. Electrons in the crystal are photo-excited when exposed to light. The spatial distribution of these excited electrons maps the intensity pattern of the incident light field. The photo-excited electrons drift out of the high intensity areas and are subsequently retrapped with an accumulation of electrons in regions of the crystal where the light intensity is less. The final result is a space charge pattern that is positive in regions of high optical intensity and negative in regions of low intensity. The space charge generates an electric field that locally modulates the index of refraction by the electro-optic effect.

To store a hologram image in the crystal (see figure), light from an argon laser is split into two beams. One of the beams is modulated by the information transparency and focused to a 2-mm spot on the crystal. The second beam (the reference beam) intersects the signal beam at the crystal. The interference pattern of the two beams is recorded. The reference beam, by itself, is used to reproduce the original signal.

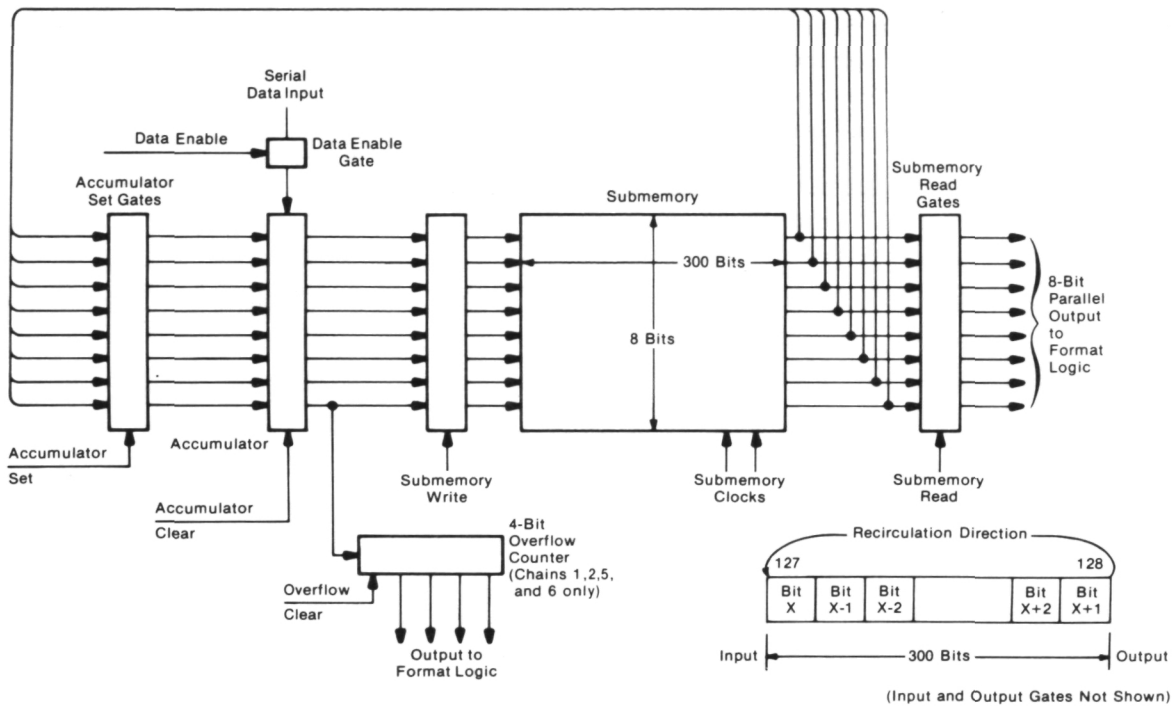
Another remarkable discovery is that the diffraction efficiency of the crystal can be increased by a factor of 2 to 5 when the same wavelength is used for readout as for storage. This discovery and the

discovery of the transition metal enhancement effect may open up many new fields in optical recording, storage, and display. Large quantities of digital information may be stored and randomly accessed for an on-line optical memory in a computer complex. TV frames, printed matter, and other optical information may be stored and processed optically.

Source: H. Aronson and
G. M. Loiacono of
Isomet Corp.
under contract to
Marshall Space Flight Center
(MFS-22348)

*Circle 23 on Reader Service Card.*

## 19.2-KILOBIT SHIFT-REGISTER MEMORY




2400-Bit Submemory and Accumulator

A multistage shift-register memory of 19.2-kilobit capacity is subdivided into 8 identical 2400-bit submemories operated in parallel. Each submemory (see figure) is associated with a particular accumulator and measurement chain. Each submemory consists of 8 parallel 300-bit shift-register chains with input and output gating; each chain is associated with one particular bit of the accumulator. Data transfers and indexing occur simultaneously throughout the memory, allowing the use of common drive signals. The eight submemory outputs are paralled, and words from individual submemories are read out sequentially. Total system volume is 262.2 $cm^3$ (16.0 $in.^3$), and the system power requirement is 58 mW.

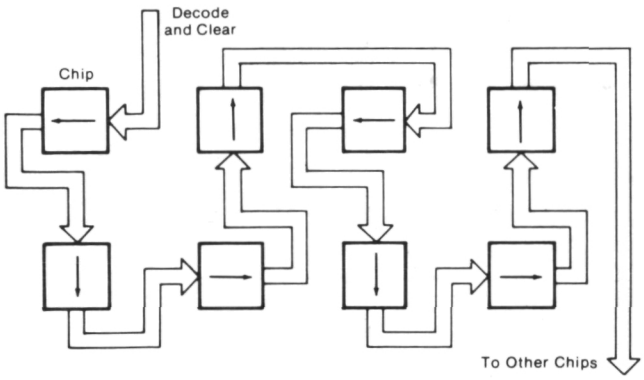
The shift-register chains are dynamic (capacitive storage) MOS logic. Data are stored as voltage levels on the gate input capacitance of each register stage or bit. The alternate application of two clock pulses transfers these voltage levels (the data) from bit to bit down the register chain.

In all dynamic registers, data must be shifted no slower than some minimum rate that is a function of MOS gate capacitance and gate leakage current. In most the minimum shift or update frequency is about 1 kHz at 25° C (77° F), or about 10 times faster than the instrument bin rate (related to the speed of the memory). For this memory a register type has been found which, because of a different substrate crystal structure, is able to operate at 100 Hz at 25° C. The incorporation of this device into the memory allows the use of bin rate updating and thereby simplifies the electrical design. Additional advantages of the memory include lower-than-usual clock and data pulse amplitudes, smaller physical size due to higher bit density per register, and cost comparable to conventional dynamic shift registers.

Source: Richard S. Taylor of
MIT Center for Space Research
under contract to
Goddard Space Flight Center
(GSC-11564)

*Circle 24 on Reader Service Card.*

## TETRAD BUBBLE DOMAIN CHIP ARRANGEMENT FOR MULTIPLEXING




Wiring Flow Diagram
for Tetrad Connection of Chips on Module

It is difficult to provide a sufficiently large number of interconnections between the chips and modules of a large bubble domain memory to yield otherwise desirable chip and memory arrangements. This problem may be overcome by using the rotating magnetic field of a bubble domain memory to obtain time-division multiplexing of the bubble domain circuits into quadrants, thus allowing four-way multiplexing on sense and control lines.

A large ($10^8$-bit) bubble domain memory can be organized or partitioned in a number of ways. One simple, straightforward approach is to divide the total memory capacity by the number of data bits per memory word (say, 64) and let the resulting storage capacity define the basic memory module. If each bit of a memory word is assigned to a different module, then only one sense amplifier per module is required. The resulting bit-per-module system is simple and has a reasonable number of interconnections per chip, module, and page (see column A of the table).

The main problem with the bit-per-module approach is that all the bubbles must be circulated all the time, resulting in a large power dissipation. The power can be reduced by circulating only a portion of the bubbles at a time. It is convenient to assemble a module from 16 chips of $10^5$ bits each. So if the memory bits were assigned on a bit-per-chip rather than a bit-per-module basis, only four modules at a time would need a rotating field supplied to them to provide access to the 64 data bits of $10^5$ words. This approach requires 32 checkbits per word, versus 8 for the bit-per-module approach, but the power is still reduced to less than one-half the original. However, since each module now requires 16 write connections and 16 sense connections, the interconnections per module and page increase drastically (see column B of the table).

MEMORY INTERCONNECTION COUNTS

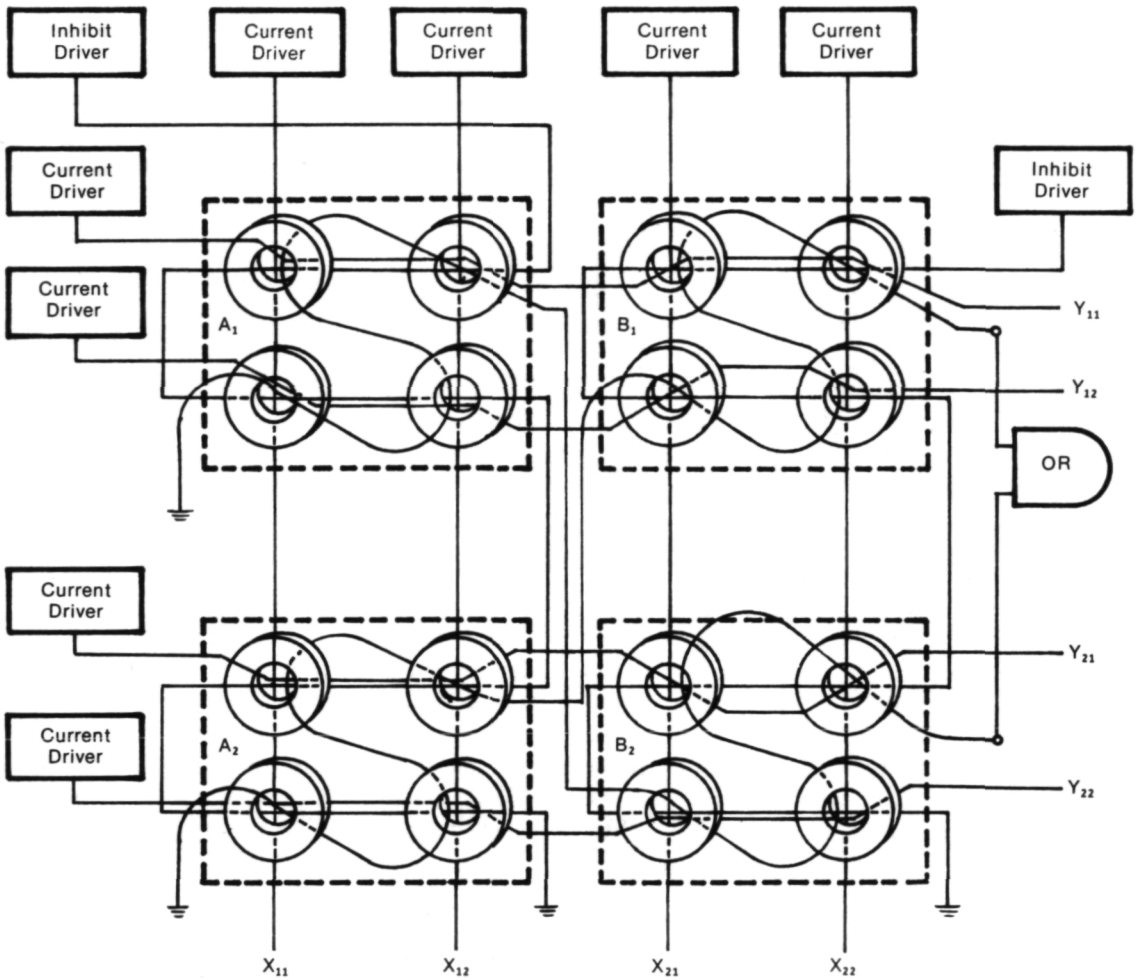
| Connections | Bit-per-Module (A) | Bit-per-Chip, Non-Tetrad (B) | Bit-per-Chip, Tetrad (C) |
|---|---|---|---|
| Per Chip | 28 | 20 | 20 |
| Per Module | 56 | 110 | 50 |
| Per Page | 68 | 411 | 123 |

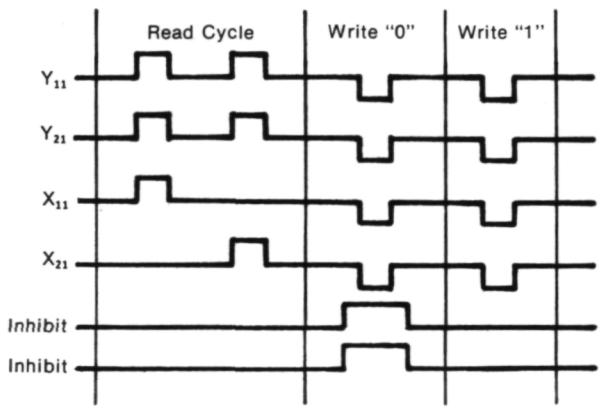
This problem can be overcome by realizing that the control currents as well as the sense signal are on for less than one quarter of the rotating field cycle. Hence, the chips can be arranged in groups of four (tetrads) at 90° to each other (see figure). The chips themselves are identical, so this space quadrature results in a time quadrature on the chips, i.e., when the first chip senses the field at 0°, the second senses it at 90°, the third senses it at 180°, and the fourth senses it at 270°. Thus at any given time only one of the four chips has a bubble opposite its sensor. This allows four-way multiplexing on the sense and control lines, which results in a significant reduction in the number of interconnections per module and page (see column C of the table) while preserving the feature of low operating power. The tetrad connection may be accomplished using no crossovers on the module, and the number of preamplifiers is reduced fourfold.

Source: G. S. Almasi of
IBM Corp.
under contract to
Marshall Space Flight Center
(MFS-22296)

*Circle 25 on Reader Service Card.*

## REDUNDANT MEMORY ORGANIZATION




Redundant Memory Organization System

In this digital information-storage technique, multiple ferrite cores are used in a redundant configuration to avoid information loss due to failed storage components or support circuitry. The technique is novel in that simultaneously copying data into quadruple memory elements provides fourfold protection against information loss. This may be useful in auxiliary long-term memory systems for large-capacity computers.

The memory organization has four redundant arrays that are interlinked by a driver and sensing and inhibit windings. A correct output is provided as long as one magnetic core of a redundant set, together with its associated driver and sensing and inhibit circuitry, has not failed. The circuitry in the figure provides a memory system in which:

a. A component failure results in no sensible output during reading or interrogation operations;
b. Redundant, single-path, magnetic-core devices are used;
c. Redundant, transfluxor, multipath, memory elements are used;
d. Redundant memory elements are arranged to tolerate coordinate-addressing current failures in a coincident-current, coordinate-selection arrangement; and
e. Redundant, magnetic memory elements provide an optimal component memory system with reliability benefits accruing from redundance.

Source: Albert W. Vinal of
IBM Corp.
under contract to
Goddard Space Flight Center
(GSC-10564)

*Circle 26 on Reader Service Card.*

## FABRICATION OF MAGNETIC BUBBLE MEMORY OVERLAY

Magnetic bubble memories are a promising improvement over the ferrite core memories used in today's computers. Magnetic bubbles use low power and have a high density of data storage. However, in order to make bubble memories economically feasible it is necessary to devise an inexpensive method of fabricating a bubble overlay. The overlay must include all the functions needed in connection with generation, propagation, sensing, and annihilation of magnetic bubble domains.

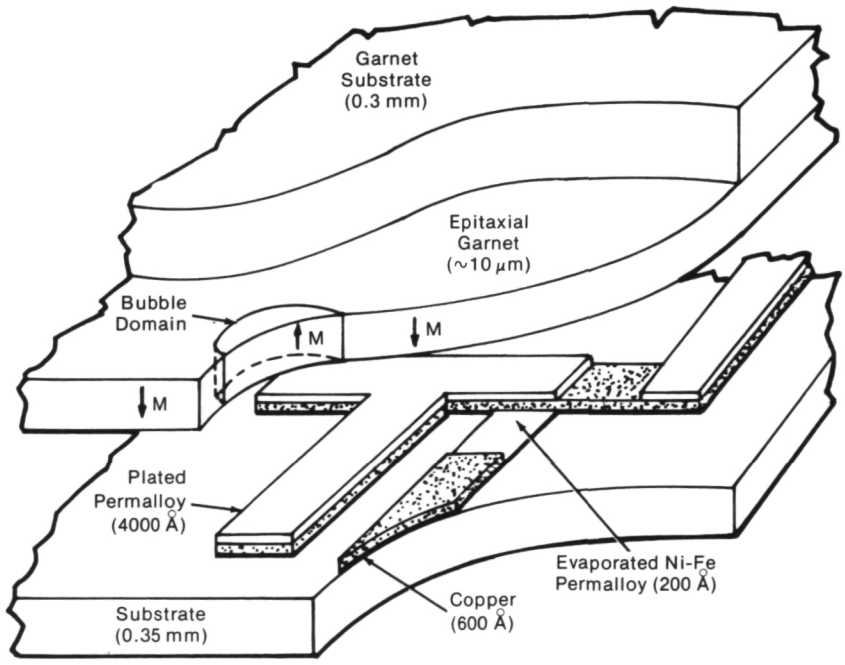
A self-contained magnetic bubble memory overlay has been fabricated by a new process that employs epitaxial deposition to form a multilayered complex of magnetically active components on a single chip. The chip structure is shown in the illustration. A glass substrate supports the overlay of thin permalloy magnetoresistive sensors, thick permalloy T-bars, and the copper (or gold) conductor lines necessary for the operation of the memory chip. A single-crystal non-magnetic garnet substrate supports the thin epitaxial magnetic garnet layer which contains the bubble domains. The chip is completed by pressing the two substrates together while a small spacing is maintained between the permalloy layer of propagation and the epitaxial garnet layer.

The overlay fabrication comprises three metal deposition steps followed by a subtractive etch. A representative sequence is as follows:

Step 1 - A 200A magnetoresistive film of Ni-Fe is deposited by evaporation onto a glass substrate in a dc in-plane magnetic field. This film is the plating surface for subsequent electro-deposition steps, and portions of it become sensors for the magnetic bubbles after the final etching.

Step 2 - The evaporated permalloy film is covered with positive photo resist ("positive" meaning that the area which has been exposed to light is removed during development). After exposure and development of the inverse of the desired conductor pattern, copper or gold conductors are electroplated in the exposed and developed-away areas.

In order to obtain a uniform conductor thickness for the overlay, the plating mask must be designed to properly balance the plated and nonplated areas. To that end, it is sometimes necessary to deposit the conductor in areas where it is not otherwise needed, but where it does not interfere with the operation of the final device.




Chip Structure

A second requirement is proper pretreatment of the evaporated permalloy film before electroforming the conductor. For otherwise, copper and gold will not, generally, adhere well to iron or iron alloys.

Step 3 - A fresh layer of positive photo resist is applied, and an inverse pattern of the thick permalloy areas (T and I bars, generators, etc.) is exposed and developed. Again the plated and nonplated areas must be balanced, and the exposed area pretreated as in Step 2.

Step 4 - The final, subtractive step serves to define the sensors and to separate the functional parts of the overlay. Three different methods can successfully remove the evaporated permalloy from unwanted areas and form the magnetoresistive sensors: chemical etching, electrochemical etching (back plating), and sputter etching.

Sputter etching gives the best yield, probably because it is the least selective and therefore easiest to control. In this method the evaporated permalloy is removed by conventional sputter-etching in an argon atmosphere. Since sputtering makes the photo-resist difficult to remove, it is left on to provide the spacing between the overlay and the bubble material and to protect against atmospheric corrosion.

Source: G. S. Almasi, R. J. Hendel,
R. E. Horstmann, T. F. Jamba, Jr.,
G. E. Keefe, S. Krongelb, J. V. Powers,
L. T. Romankiw, and L. L. Rosier of
IBM Corp.
under contract to
Marshall Space Flight Center
(MFS-22377)

*Circle 27 on Reader Service Card.*

# Patent Information

The following innovations, described in this Compilation, have been patented or are being considered for patent action as indicated below:

**Television Noise-Reduction Device** (Page 1) MSC-12607

This innovation has been patented by NASA (U.S. Patent No. 3,875,584).

and

**Phase Shift Keyed, Pulse Code Modulated Signal Synchronizer** (Page 22) MSC-12462

This innovation has been patented by NASA (U.S. Patent No. 3,800,227).

and

**Pulse Stretcher for Narrow Pulses** (Page 24) MSC-14130

This innovation has been patented by NASA (U.S. Patent No. 3,831,098).

Information concerning nonexclusive or exclusive license for the commercial development of the three inventions above should be addressed to:

Patent Counsel
Johnson Space Center
Code AM
Houston, Texas 77058

**Numerical Interactive Controller** (Page 8) NPO-11497

This invention has been patented by NASA (U.S. Patent No. 3,729,129). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
NASA Pasadena Office
4800 Oak Grove Drive
Pasadena, California 91103

**A Magnetically Focused Image Tube Employing an Opaque Photocathode** (Page 10) GSC-11602

This invention has been patented by NASA (US. Patent No. 3,806,756), and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
Goddard Space Flight Center
Code 204
Greenbelt, Maryland 20771

**Signal Acquisition From Charge-Storage-Mode Photosensor Arrays** (Page 12) MFS-22629

and

**Laser Addressed Holographic Memory System** (Page 29) MFS-22565

and

**A New Optical Recording Medium** (Page 32) MFS-22348

Inquiries concerning rights for the commercial use of these inventions should be addressed to:

Patent Counsel
Marshall Space Flight Center
Code CC01
Marshall Space Flight Center, Alabama 35812

**Solid-State Converter for Measurements of Aircraft Noise and Sonic Boom** (Page 17) LAR-11173

This invention has been patented by NASA (U.S. Patent No. 3,868,856). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
Langley Research Center
Mail Stop 313
Hampton, Virginia 23665

**Low Phase-Noise Digital Frequency Divider** (Page 18) NPO-11569

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
NASA Pasadena Office
4800 Oak Grove Drive
Pasadena, California 91103

**High Speed Direct-Binary to Binary-Coded-Decimal Converter and Scaler** (Page 20) KSC-10326

This invention has been patented by NASA (U.S. Patent No. 3,638,002). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
Kennedy Space Center
Code AD-PAT
Kennedy Space Center, Florida 32899

**RF-to-Digital Converter** (Page 26) MSC-14419

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457(f)], to the General Electric Company, 1830 NASA Blvd., Houston, Texas 77058.

**An Improved Holographic Recording Medium** (Page 28) MFS-22532

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457(f)], to the RCA Corp., Princeton, New Jersey 08540.

**Fabrication of Magnetic Bubble Memory Overlay** (Page 38) MFS-22377

and

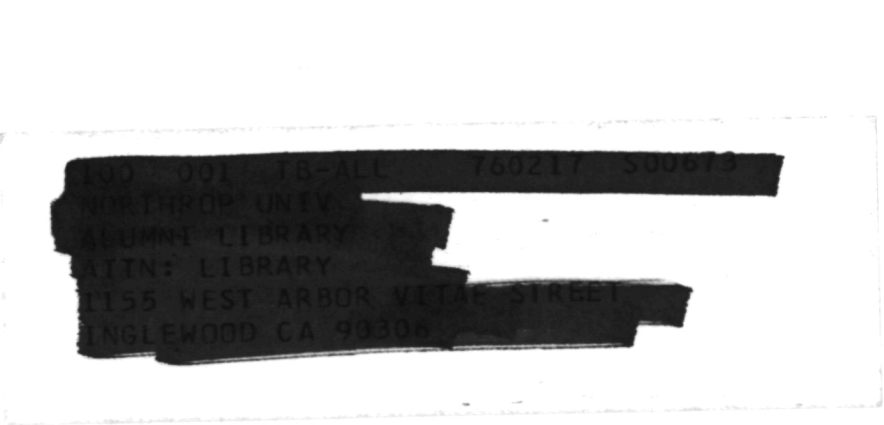
**Tetrad Bubble Domain Chip Arrangement for Multiplexing** (Page 35) MFS-22296

Titles to these inventions have been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457(f)], to the IBM Corp., Huntsville, Alabama 35805.

**Laser-Actuated Holographic Storage Device** (Page 30) MFS-22768

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457(f)], to the David Sarnoff Research Center, Princeton, New Jersey 08540.

U.S. Government Printing Office: 1976-638-153 Region 3-II




*"The aeronautical and space activities of the United States shall be conducted so as to contribute . . . to the expansion of human knowledge of phenomena in the atmosphere and space. The Administration shall provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof."*

—NATIONAL AERONAUTICS AND SPACE ACT OF 1958

# NASA TECHNOLOGY UTILIZATION PUBLICATIONS

These describe science or technology derived from NASA's activities that may be of particular interest in commercial and other non-aerospace applications. Publications include:

TECH BRIEFS: Single-page descriptions of individual innovations, devices, methods, or concepts.

TECHNOLOGY SURVEYS: Selected surveys of NASA contributions to entire areas of technology.

OTHER TU PUBLICATIONS: These include handbooks, reports, notes, conference proceedings, special studies, and selected bibliographies.

*Details on the availability of these publications may be obtained from:*

National Aeronautics and
Space Administration
Code KT
Washington, D.C. 20546

Technology Utilization publications are part of NASA's formal series of scientific and technical publications. Others include Technical Reports, Technical Notes, Technical Memorandums, Contractor Reports, Technical Translations, and Special Publications.

*Details on their availability may be obtained from:*

National Aeronautics and
Space Administration
Code KS
Washington, D.C. 20546

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Washington, D.C. 20546